

PAGE	TITLE
01	INDEX
02	BLOCK DIAGRAM
03	CLOCKS DIAGRAM
04	POWER DISTRIBUTION DIAGRAM
05	POWER FLOW DIAGRAM
06	STRAP & GPIO
07	POWER SEQUENCE DIAGRAM
08	INTERRUPT & PME DIAGRAM
09	CPU XDP
10	MCP- CLK/CTRL/MISC/DEBUG
11	MCP- DDR4 CHANNEL A & B
12	MCP- PCI/DMI/DDI
13	MCP- POWER CONNECTIONS
14	MCP- VSS
15	BLANK
16	DDR4 CHA D0 XIMM4
17	DDR4 CHA D1 XIMM3
18	DDR4 CHB D0 XIMM2
19	DDR4 CHB D1 XIMM1
20	PCH - DMI/PCIE/USB2-3
21	PCH - SMBUS/HDA/GPIO/JTAG
22	PCH - SATA/SPI/GPIO
23	PCH - GPIO/MISC
24	PCH - CLOCK
25	PCH - PWR/STRAP
26	PCH-PLL FILTER & DECOUPLING
27	SIO_A
28	SIO_B
29	M2_SSD_SOCKET3(Z2 Only)
30	AUDIO CODEC
31	AUDIO SPEAKER OUT
32	TPM & METS/APS
33	FP & DSW LOGIC
34	SPI EEPROM
35	PWR CON/AUXLED/PCB
36	FAN HEADERS/PSU PIN
37	Intel Jacksonville
38	SATA/PS2/CMOS
39	USB POWER
40	REAR/RJ45/MEDIA USB
41	FRONT USB/HEADER
42	USB CHARGER
43	PCIE - x16
44	PCIE - x1
45	PCIE - x4
46	DP2VGA
47	DISPLAY PORT 1(SINGLE)
48	DISPLAY PORT 2(DUAL-C)
49	DISPLAY PORT 2(DUAL-D)
50	COMA/COMB/SCSI
51	BLANK
52	LEDs/HOODLOCK_SENSE
53	FEATRUES
54	+12V_DUAL
55	+3P3V_LPS
56	System Power
57	+5V_GPIO
58	+1P8V_+3P3V_PCH_GPPA
59	+1V_PCH
60	+1P2V_SFROC
61	+VPP
62	+1P2V_VDDQ
63	+VTT_DDR
64	+5V_MAIN & +3P3V_MAIN
65	+VCCIO
66	+VCCSA
67	+VCORE VGT CONTROLLER
68	+VCORE PHASE 1 & 2
69	+VCORE PHASE 3
70	+VGT Phase 1 & 2
71	USB POWER/FAN(Z2 Only)
72	Changelist

Intel SkyLake Plat f o r m

SLK-S CPU / SLK PCH-H

BOM DISTRIBUTION RULE
Spitfire, Scorpion, Toledo, Bunun
(BOM,BOM,BOM, BOM)

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Marking	Description
I	Installed
NI	Not Installed
MP	Production Part ONLY
PROTO	Not For Production Part
CCL	Critical Components List

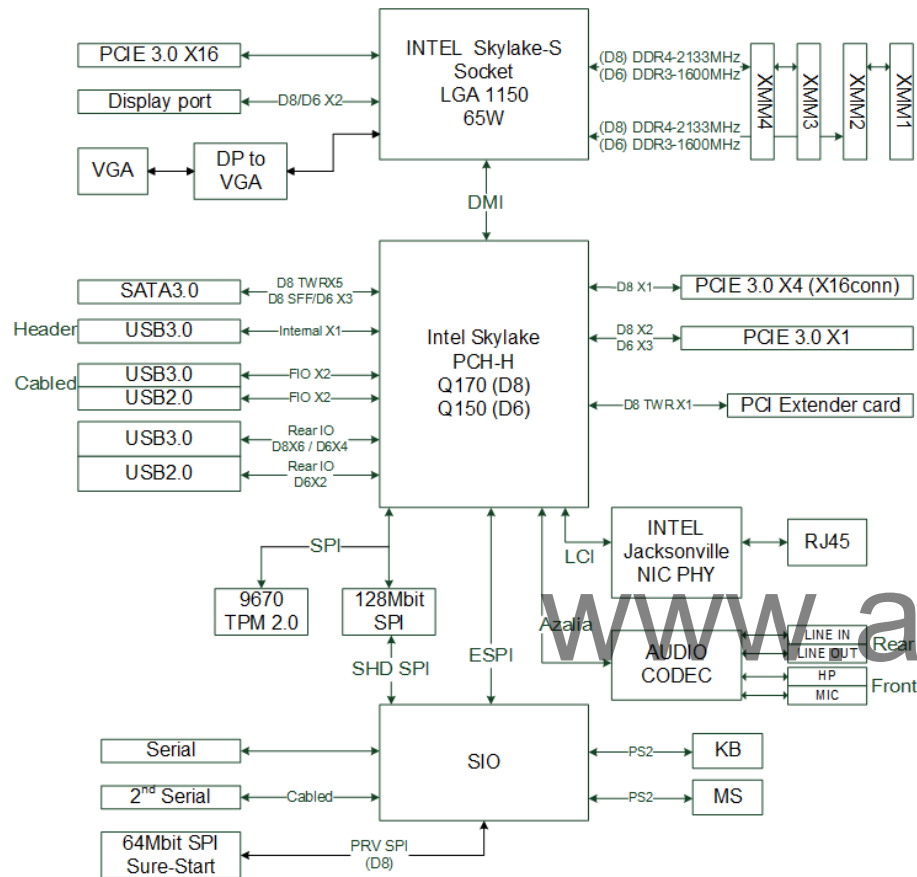
PCB AND SILKSCREEN COLOR		
Program Phase	Color of PCB	Silkscreen
DB1 (Design Build)	RED	YELLOW
DB2+	RED	WHITE
SI1 (System Integration)	LIGHT BLUE	YELLOW
SI2+	LIGHT BLUE	WHITE
PV1 (Production Validation)	GREEN	YELLOW
PV2+	GREEN	WHITE
MVB / PRODUCTION	GREEN	WHITE

	Spitfire	Scorpion	Toledo	Bunun
PCH	Q170	Q170	Q150	C236

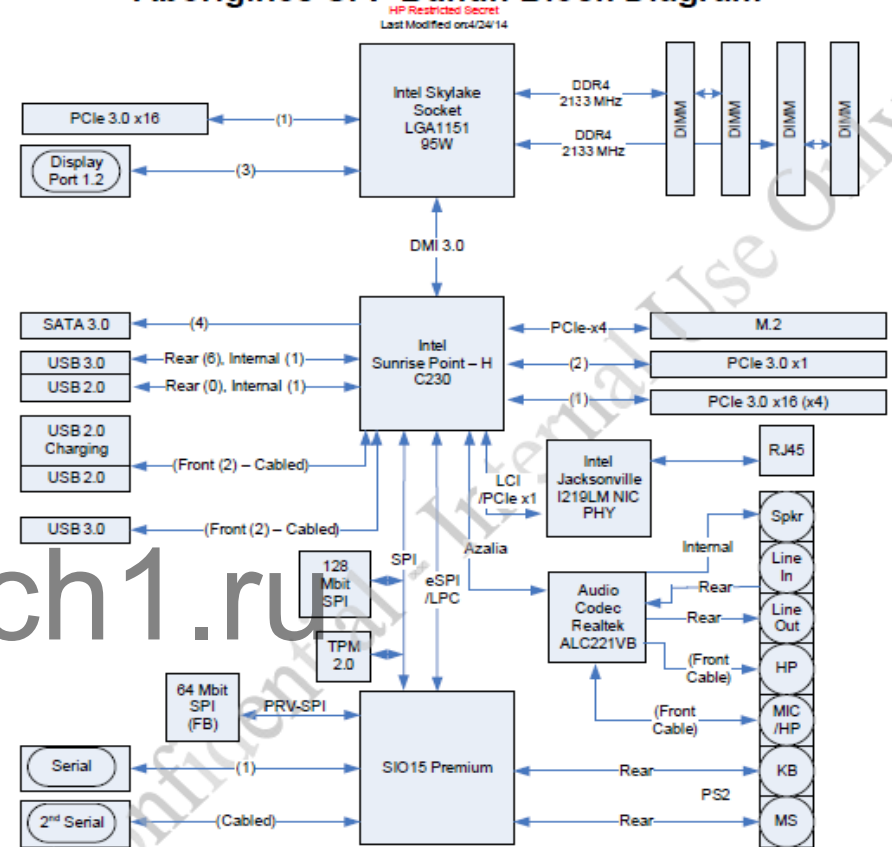
PCA P/N, Spitfire/Scorpion/Toledo/Bunun	795206-001/ 795206-002/ 795231-001/ 795003-001
SCH P/N, Spitfire/Scorpion/Toledo/Bunun	795207-000/ 795207-000/ 795207-000/ 795207-000
PCB P/N, Spitfire/Scorpion/Toledo/Bunun	795208-001/ 795208-001/ 795208-001/ 795208-001

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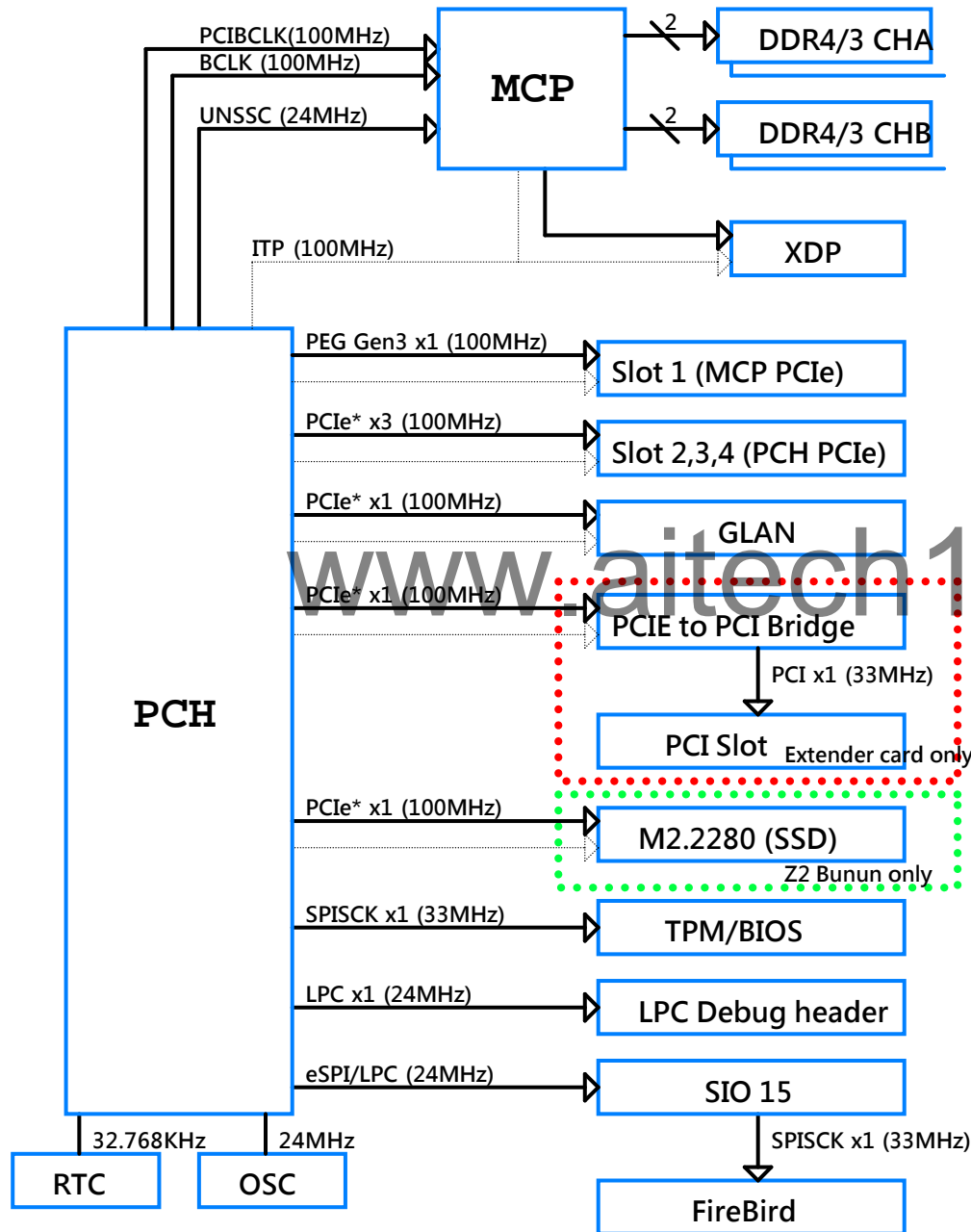
Aborigines SFF Bunun Block Diagram




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Clock Diagram



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Custom	795207-000				
Date:	Monday, June 29, 2015		Sheet	3 of 72	

POWER SUPPLY
+12V_CPU
+12V
-12V
+12V_AUX

VBAT 3.0
VCCRTC

+12V_CPU
+12V_DAUL

BATT1

CPU Core Switcher
3+2phase Switching
+VCCIA 63A 0V - 1.52V
+VCCGT 37A 0V - 1.52V

VCCSA Switcher
11A 1.05V

VCCIO Switcher
5.5A 0.95V

VCC_DDR Switcher
12.14A 1.2V

+VPP
2.24A 2.5V

+1.0V_PCH
10.66A 1.0V

+1P8V_+3P3V_PCH_GPPA Switcher
0.4A 1.8V

5V & 3.3V Switcher
+5V_AUX
14.462A
+3P3V_AUX
17.16

+3.3V_LPS
0.502A (LPS:0.00206A)

+VCCIA

+VCCGT

+VCCSA

+VCCIO

+VDDQ

+VPP

+1.0V_AUX

+VDDQ

+VPP

+1.0V_AUX

PIV8_P3V3_PCH_GPPA

+5V_AUX/+5V_DUAL/+5V_MAIN/+5V_GPIO

+3P3V_AUX/+3P3V_MAIN

+3.3V_LPS

+VDDQ

+VPP

+1.0V_AUX

PIV8_P3V3_PCH_GPPA

+5V_AUX/+5V_DUAL/+5V_MAIN/+5V_GPIO

+3P3V_AUX/+3P3V_MAIN

+3.3V_LPS

+5V

+12V

+3P3V_AUX

+5V_DUAL

+3.3V_AUX

+3.3V_MAIN

+12V

+5V_DUAL

PARALLEL PORT
15mA 75mW

SERIAL PORT
1mA 12mW
50uA 165uW

PS2 KB/M
50mA 250mW

PCIE SLOT x4
0.375A 1.2375W
9A 29.7W
9.7A 116.4W

USB PORT x11
3.0 X9 2.0 X2
9.1A 45.5W

+VCCIA

+VCCGT

+VCCSA

+VCCIO

SLK (65W TDP)

79A

45A

11.1A

5.5A

+1.0V_AUX

PIV8_P3V3_PCH_GPPA

+3.3V_AUX

+3.3V_LPS

+3P3V_MAIN

+3V_BATT

SKL-S (5.92W TDP)

9.948A 9.948W

0.038A 0.0684W

0.633A 2.0889W

0.204A 0.6732W

7mA 23.1mW

1mA 3.3mW

+3.3V_AUX

+3V_BATT

+3.3V_LPS

+SIO_SPI_POWER

+IPQV_VCCST

PIV8_P3V3_PCH_GPPA

SUPER I/O

95mA 313.5mW

1.5uA 3.3uW

10uA 33uW

30mA 99mW

10mA 10mW

10mA 33mW

+12V

+5V

HARD DRIVER

0.35A 4.2W

0.72A 3.6W

+12V

+5V

CD ROM

1.5A 18W

1.5A 7.5W

+12V

FAN

200mA 2.4W

+VDDQ

+VPP

DDR4 DIMM x4
12A 14.4W
1A 0.6W

+5V_AUX

+3.3V_AUX

AUDIO

33mA

33mA

+3.3V_AUX

SPI EEPROM

30mA 0.1W

+3.3V_LAN

LAN

542mW

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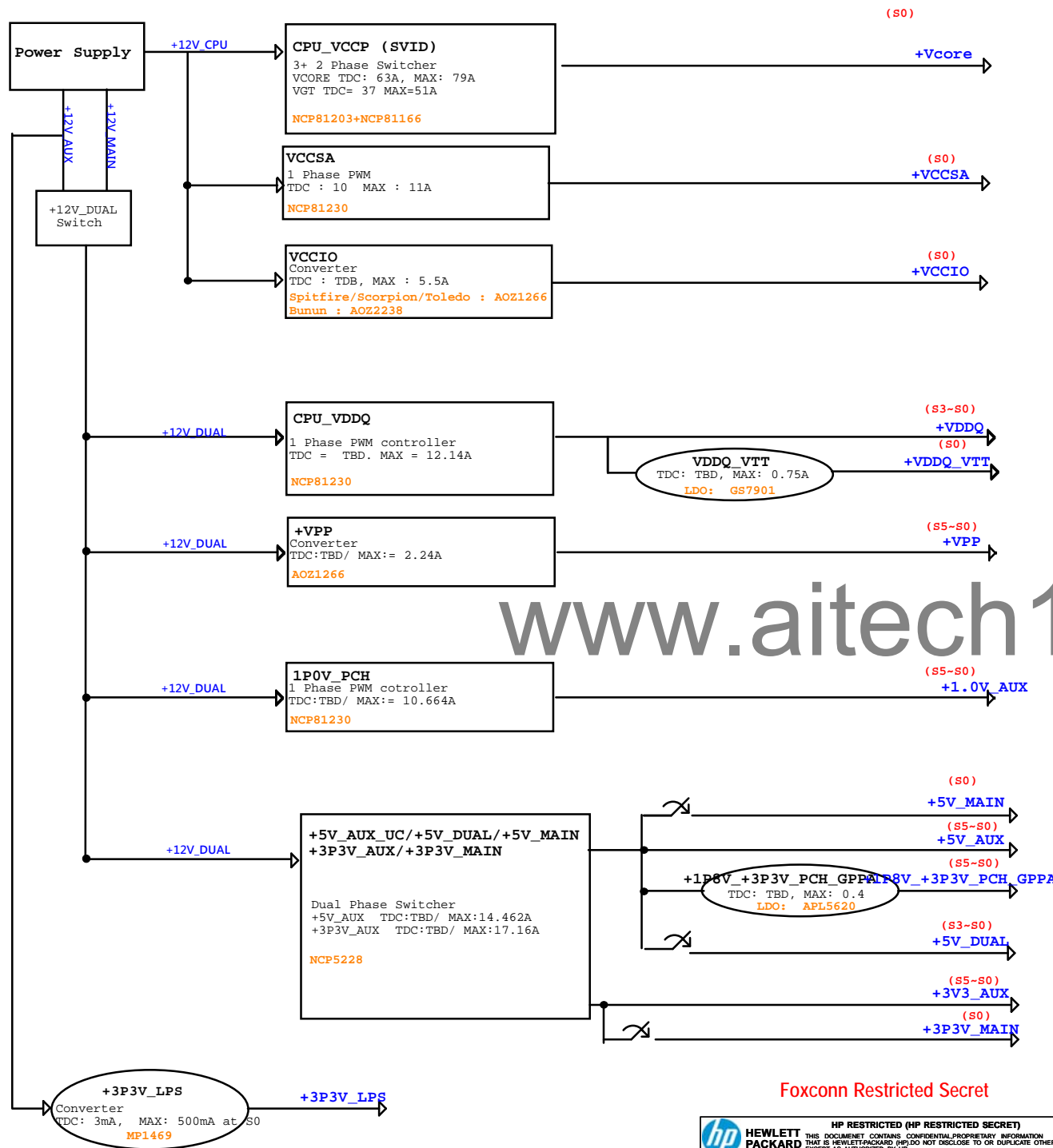
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8



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I(*) means used to enable the interval PD by ECM


I(*) means used to enable the interval FD by ROME

I(9) means need to enable the interval 90 by 8000I(*) must be used to enable the internal PD by SIG

I(F) means used to enable the interval FO by RDS

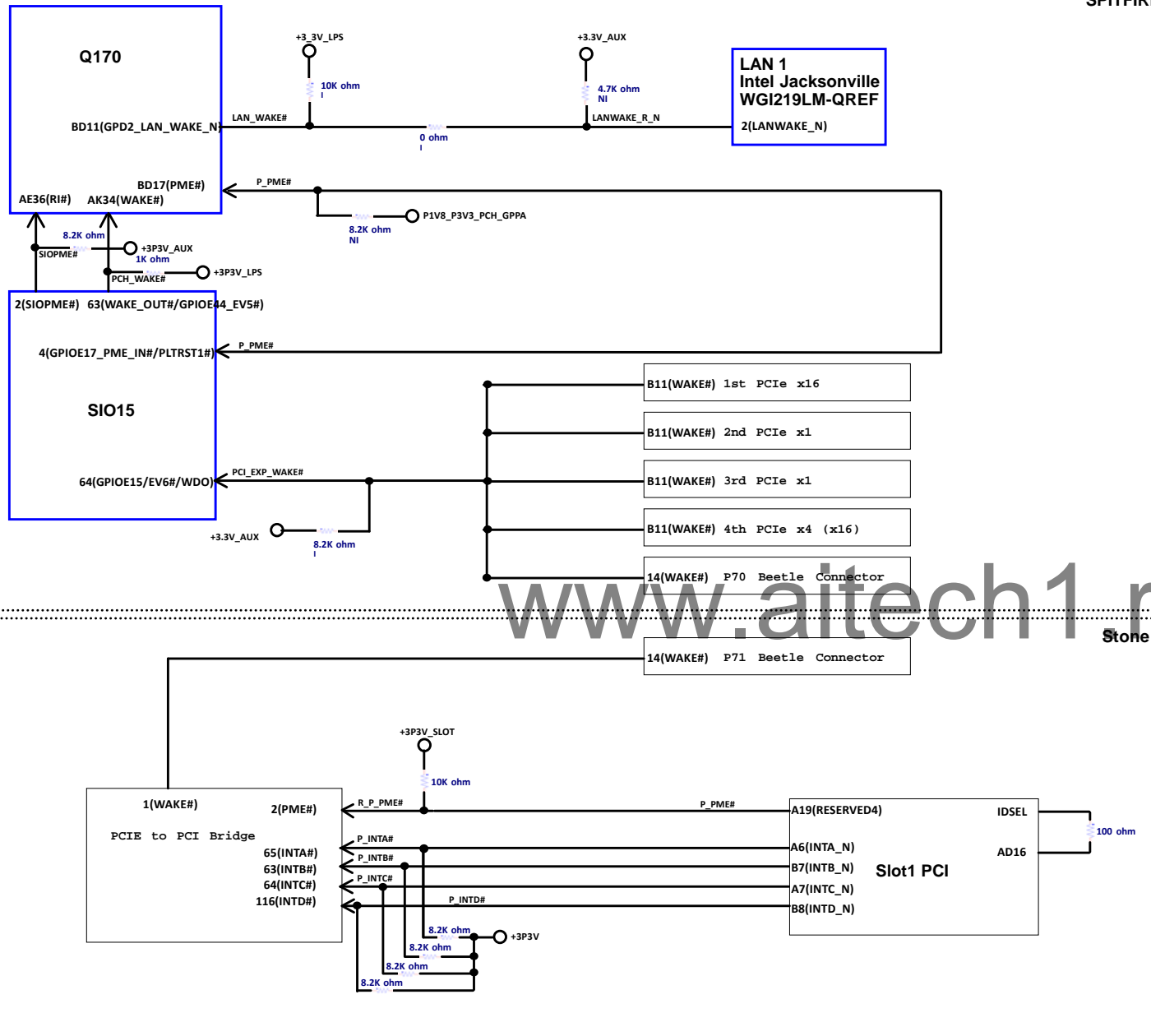
The diagram shows the timing of various signals during the transition from S5 to S0. The signals are listed on the left, and their transitions are shown as waveforms. Key events and annotations include:

- SLP_S4#**: SIO receives PWRRTIN#, and send PWRRTOUT# to PCH. After that, PCH generates SLP_S4#, SLP_S3#.
- SLP_S3#**: SIO receives SLP_S3# and other signals, generating PSON#.
- PSON#**: 25ms delay.
- +12V**: Source: +12V_DUAL.
- +12V_DUAL**: Source: +12V_DUAL.
- +VPP**: Source: +12V_DUAL.
- +VDDQ/VCCPLL OC**: Source: +12V_DUAL.
- DDR_PGOOD**: Source: +12V_DUAL.
- +5V_MAIN**: Source: +12V_DUAL.
- +3.3V_MAIN**: Source: +12V_DUAL.
- +VCCIO**: Source: +12V_CPU.
- +VCCIO_PGOOD**: Source: +12V_CPU.
- +VCCSA**: Source: +12V_CPU.
- +VCCSA_PGOOD**: TBD: Earlier or later than 30ms.
- PWRGD_30MS**: 30ms delay.
- PWRGD_140MS**: 140ms delay.
- VCORE_EN**: Feed into PCH PCH_PWRGD.
- +VCCIA**: Depending on SLP_S3# & PWRGD_30MS & +VCCSA_PWRGD.
- VCORE_PG**: IMVP8: 5us.
- SYS_PWROK**: IMVP8: 500ns (After VCORE_EN).
- VCCST_PWRGD**: CPU will assert DDR_VTT_CNTRL after VCCST_PWRGD crosses its threshold point.
- DDR_VTT_CNTRL**: Source: +3.3V_AUX.
- +VTT**: +VCCGT and +VCCIA used the same power controller.
- +VCCGT**: PLTRST# active to PROC_PWRGD inactive.
- H_PWRGOOD**: Indication to CPU that VCC and Clock are stable.
- PLTRST#**: [tPCH33] Max: 99ms.

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Interrupt & PME diagram

SPITFIRE




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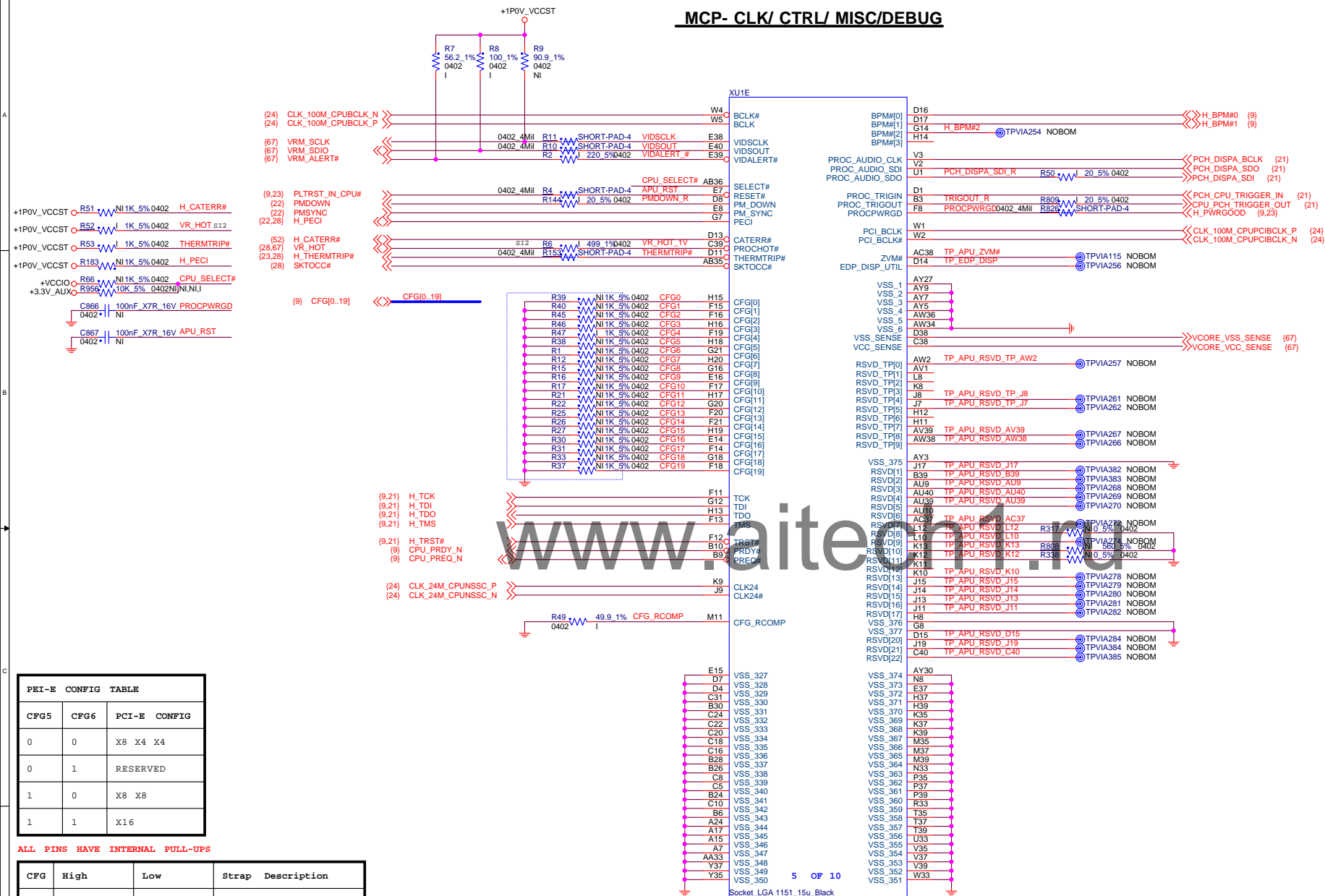
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I: R880/R881/R882/R883/R884/R885/R781/R782



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Rev A	

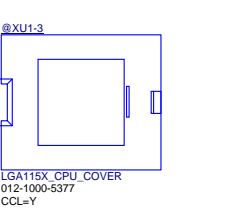
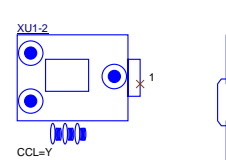
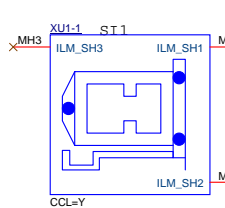
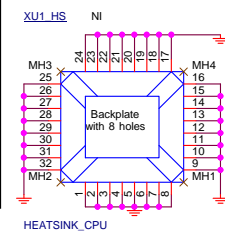
MCP- CLK/ CTRL/ MISC/DEBUG



PEI-E CONFIG TABLE		
CFG5	CFG6	PCI-E CONFIG
0	0	X8 X4 X4
0	1	RESERVED
1	0	X8 X8
1	1	X16

ALL PINS HAVE INTERNAL PULL-UPS

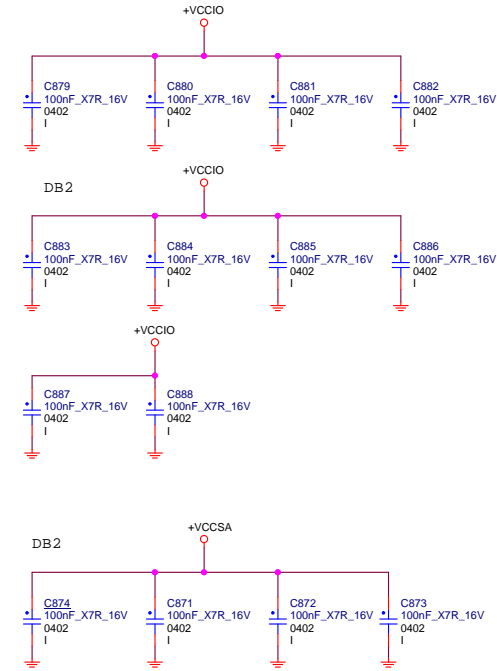
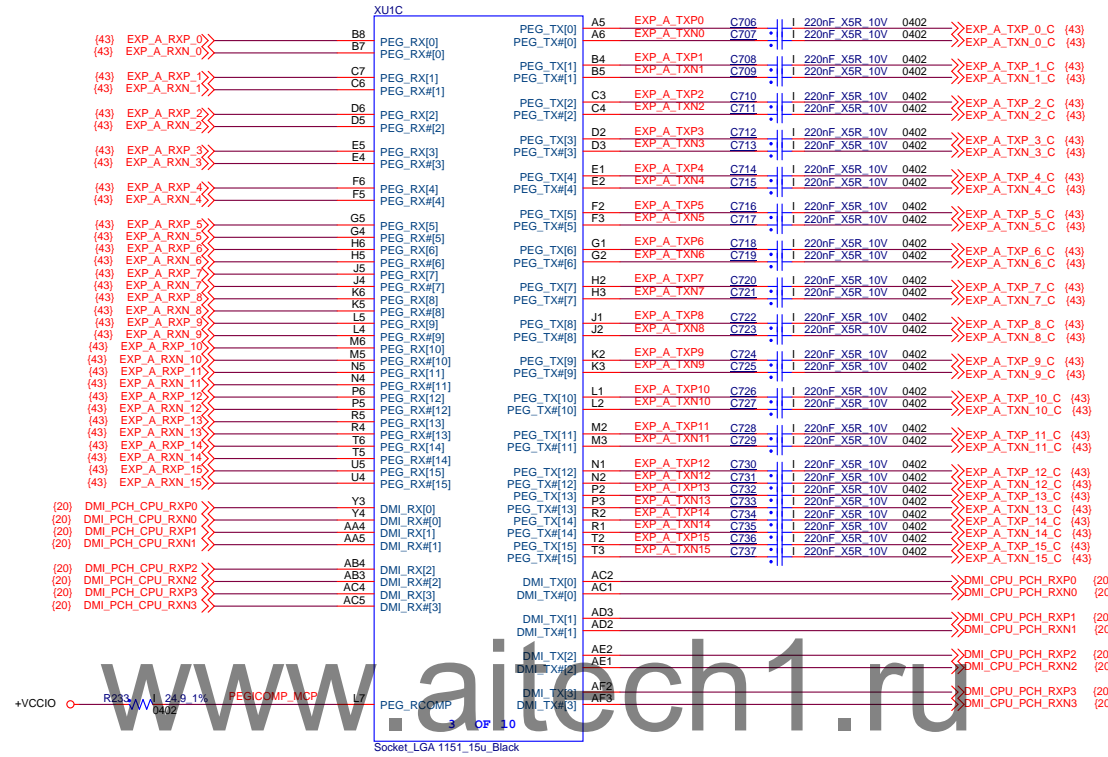
CFG	High	Low	Strap Description
0	NORMAL	STALL	EAR
1		REVERSE	RESERVED
2	NORMAL	REVERSE	PEG LANE REVERSAL
3		REVERSE	RESERVED
4	DISABLE	ENABLE "0"	eDP enable
5	DISABLE "1"	DISABLE "1"	PEG0CFGSEL[0] x16
6	DISABLE "1"	DISABLE "1"	PEG0CFGSEL[1] x16
7	RESET N	BIOS REQ	PEG DEFER TRAINING
8-19			RESERVED



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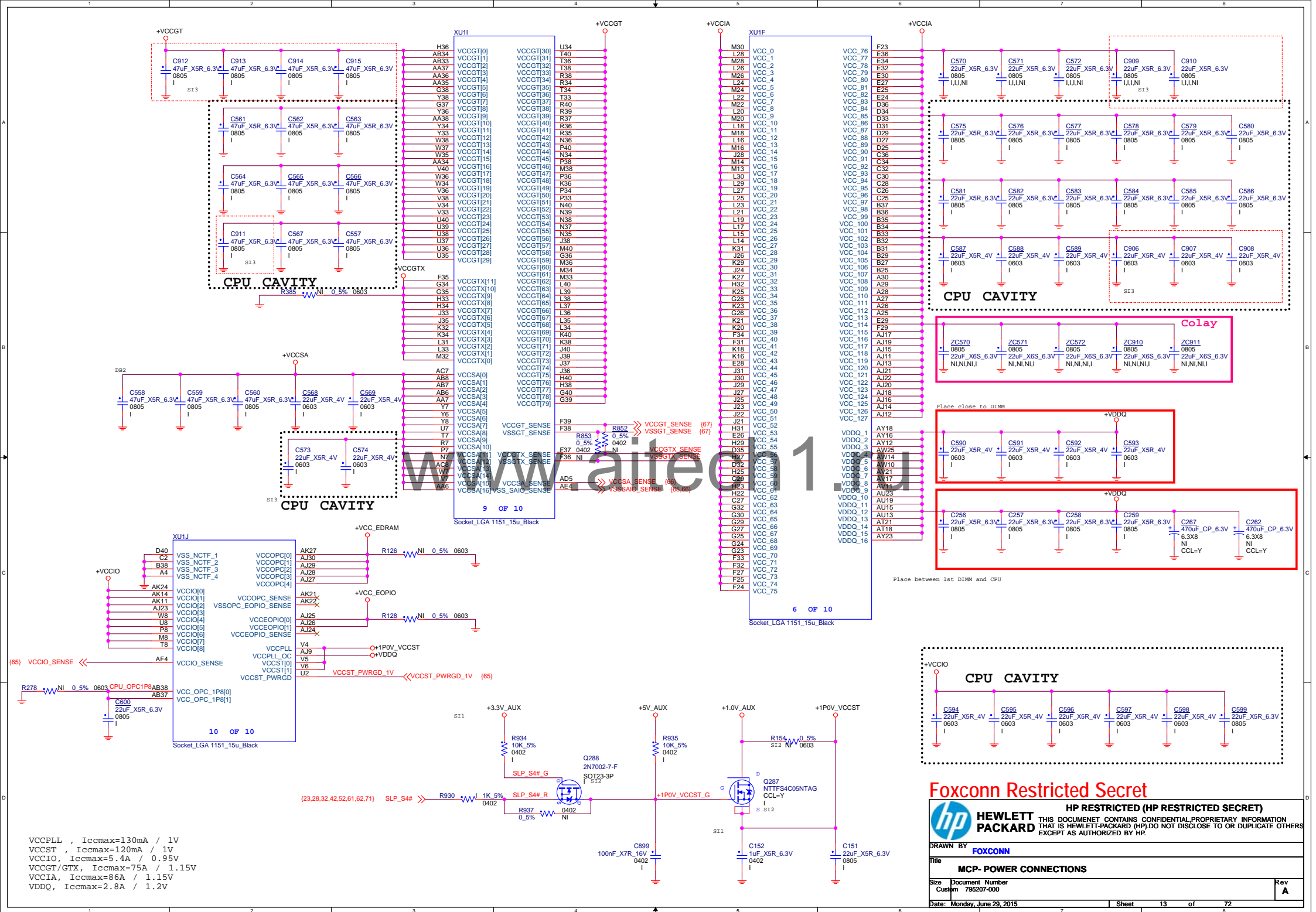
hp		HEWLETT PACKARD		HP RESTRICTED (HP RESTRICTED SECRET)	
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Date:	Monday, June 29, 2015	Sheet	10	of	72

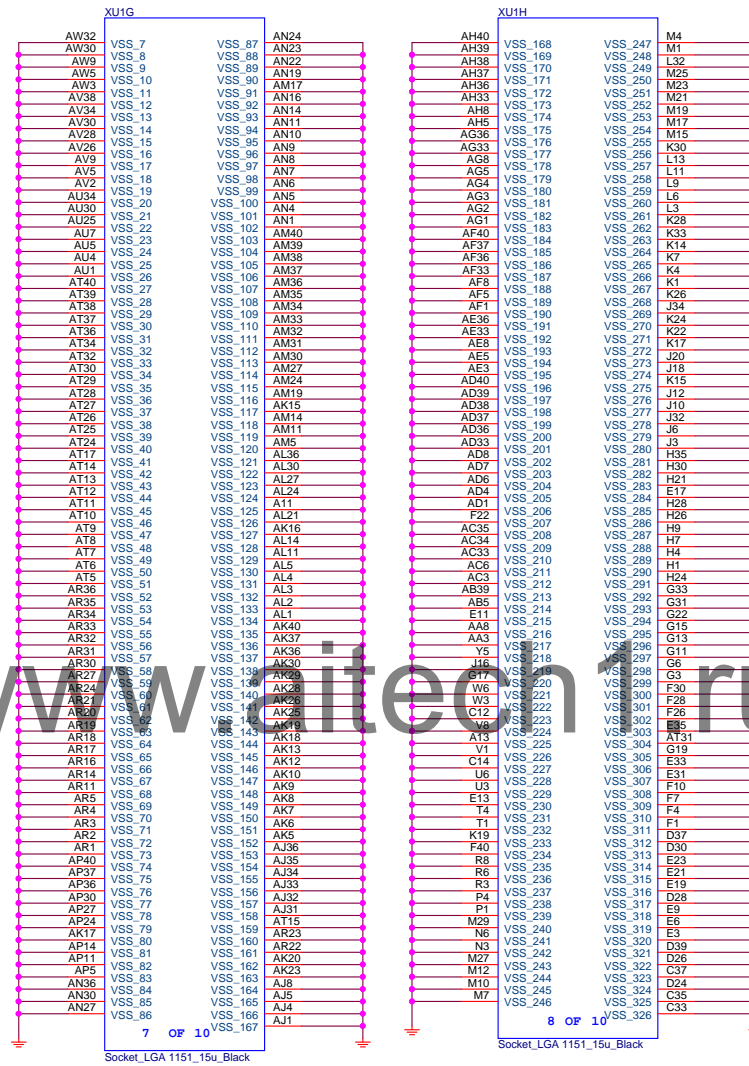
MCP - PCIE,DMI,FDI,DDI




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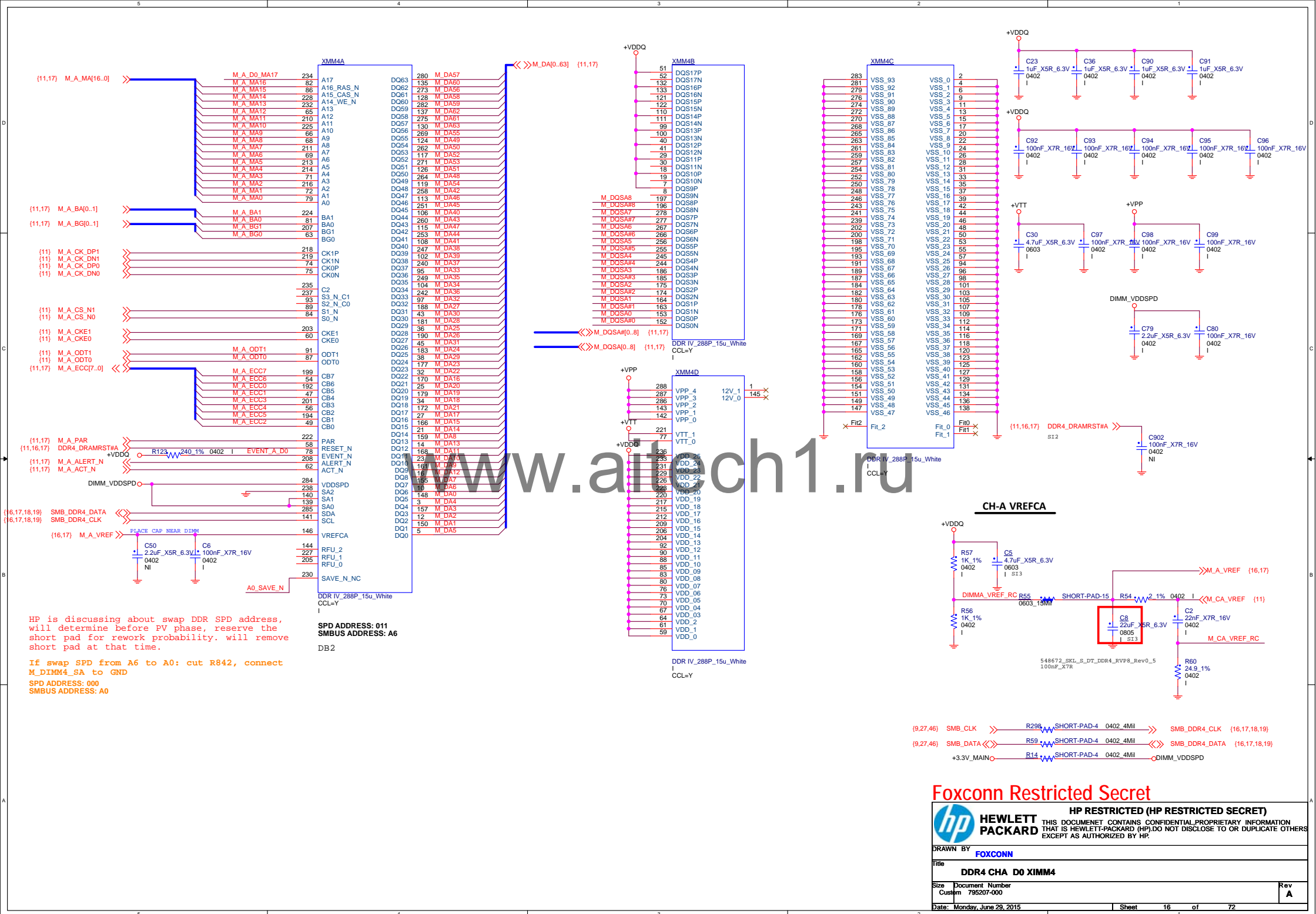
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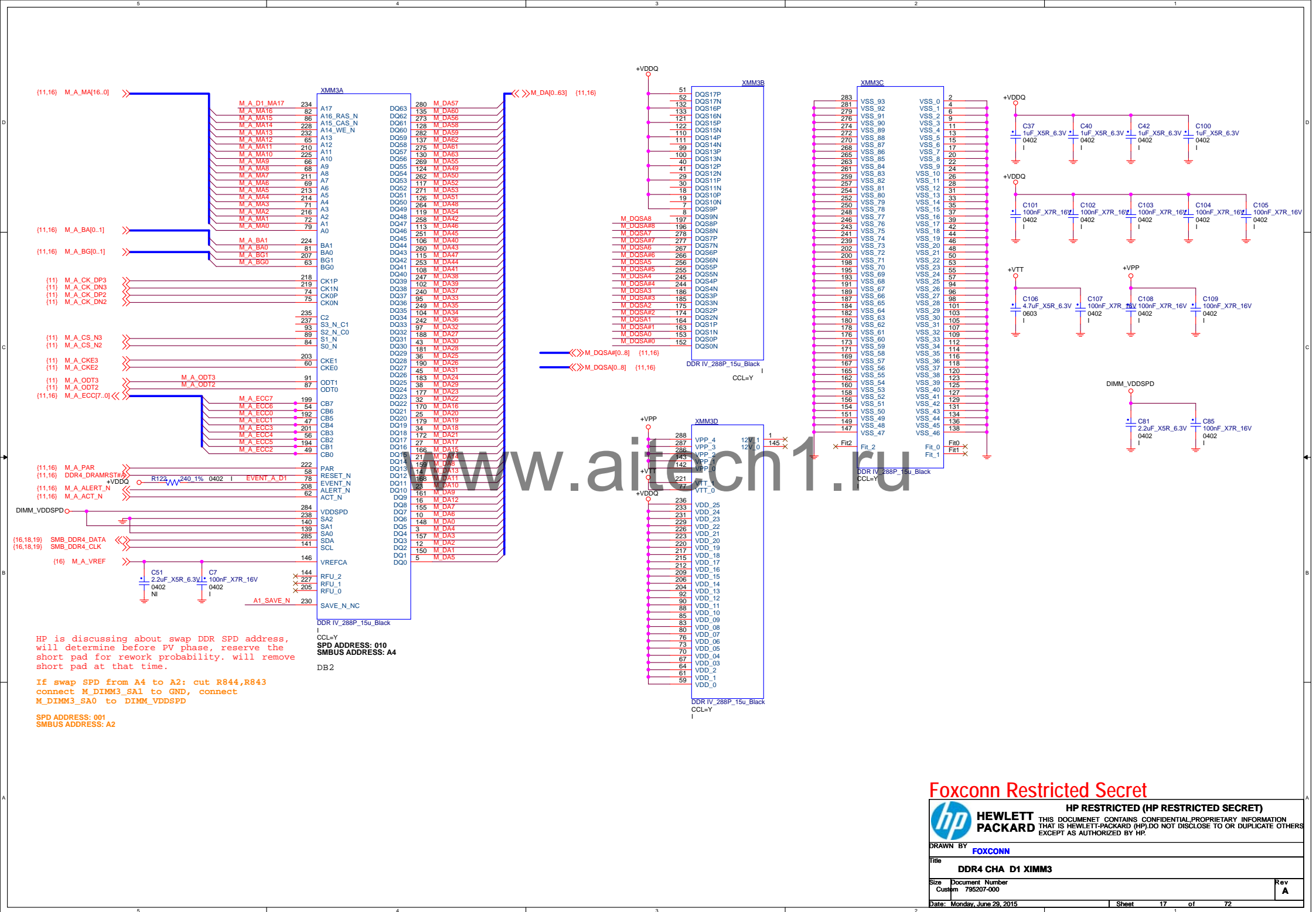
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Date: Monday, June 29, 2015		Sheet	15	of	72





HP is discussing about swap DDR SPD address, will determine before PV phase, reserve the short pad for rework probability. will remove short pad at that time.

If swap SPD from A4 to A2: cut R844,R843 connect M_DIMM3_SA1 to GND, connect M_DIMM3_SA0 to DIMM_VDDSPD

SPD ADDRESS: 001
SMBUS ADDRESS: A2

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Title

DDR4 CHA D1 XIMM3

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Monday, June 29, 2015

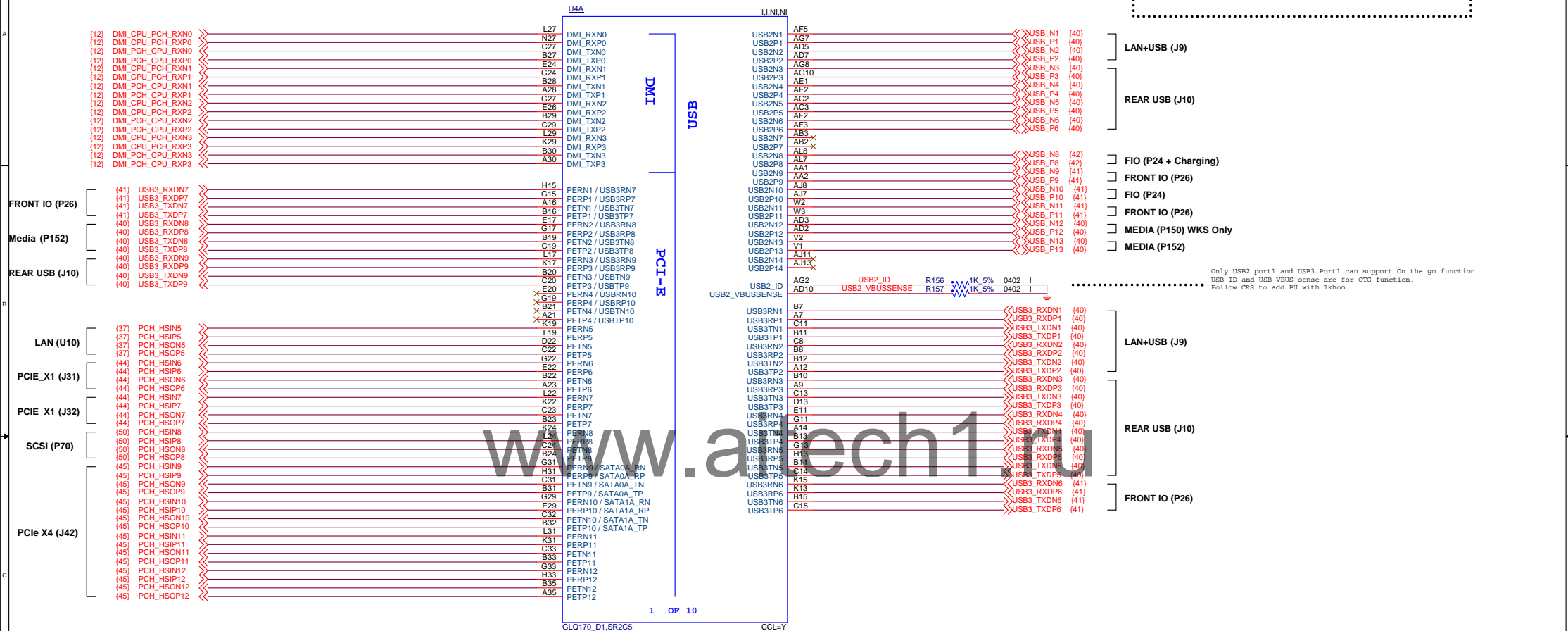
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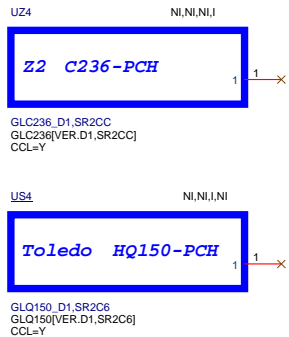
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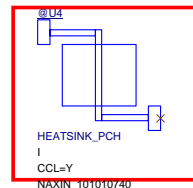
USB3 and USB2 port mapping is not clear in PDG.
Have to check again if Intel releases new PDG.



Only USB2 port1 and USB3 Port1 can support On the go function
USB ID and USB VBUS sense are for OTG function.
Follow CRB to add PU with 1kOhm.



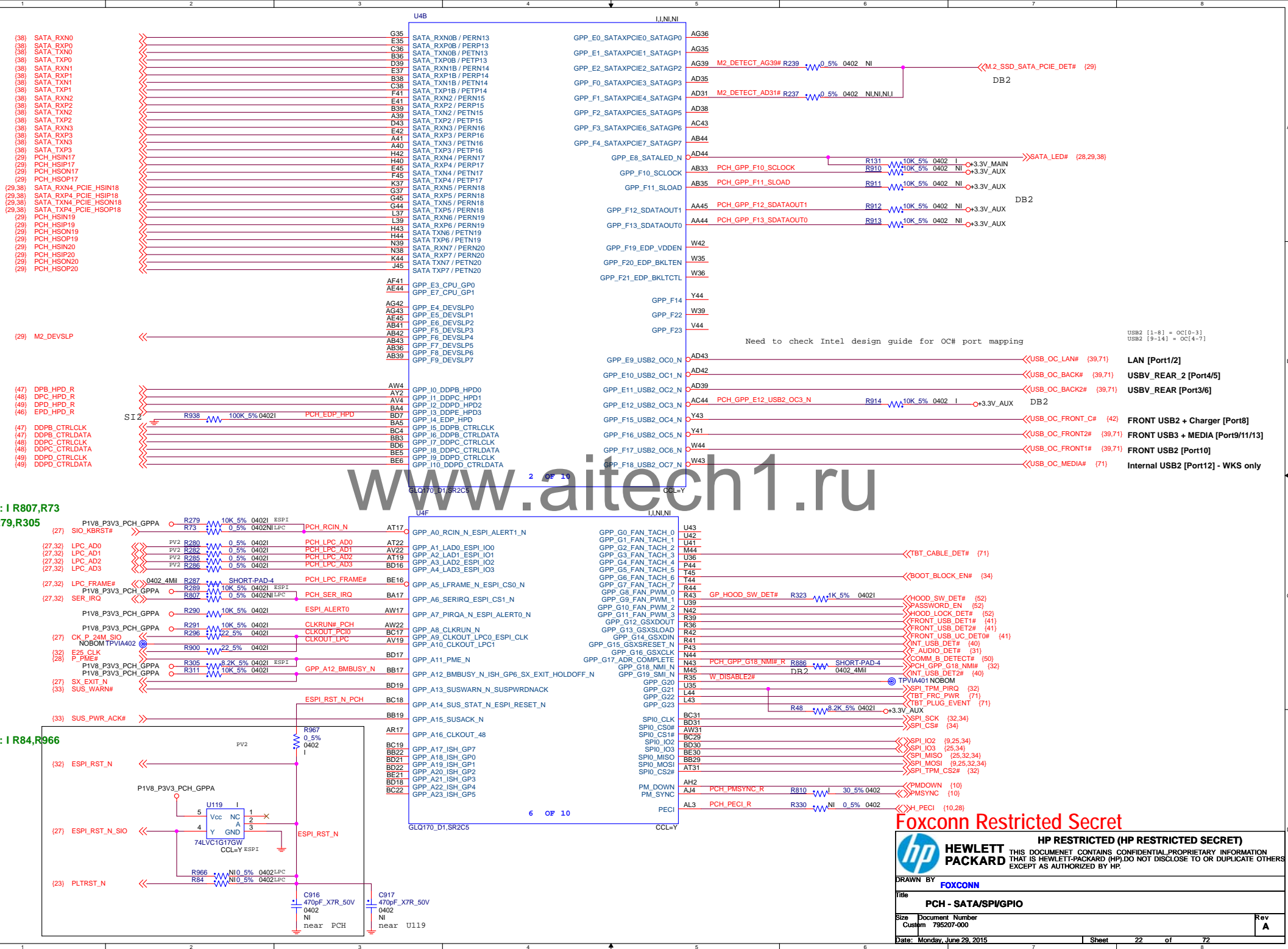
Check PCH HS size



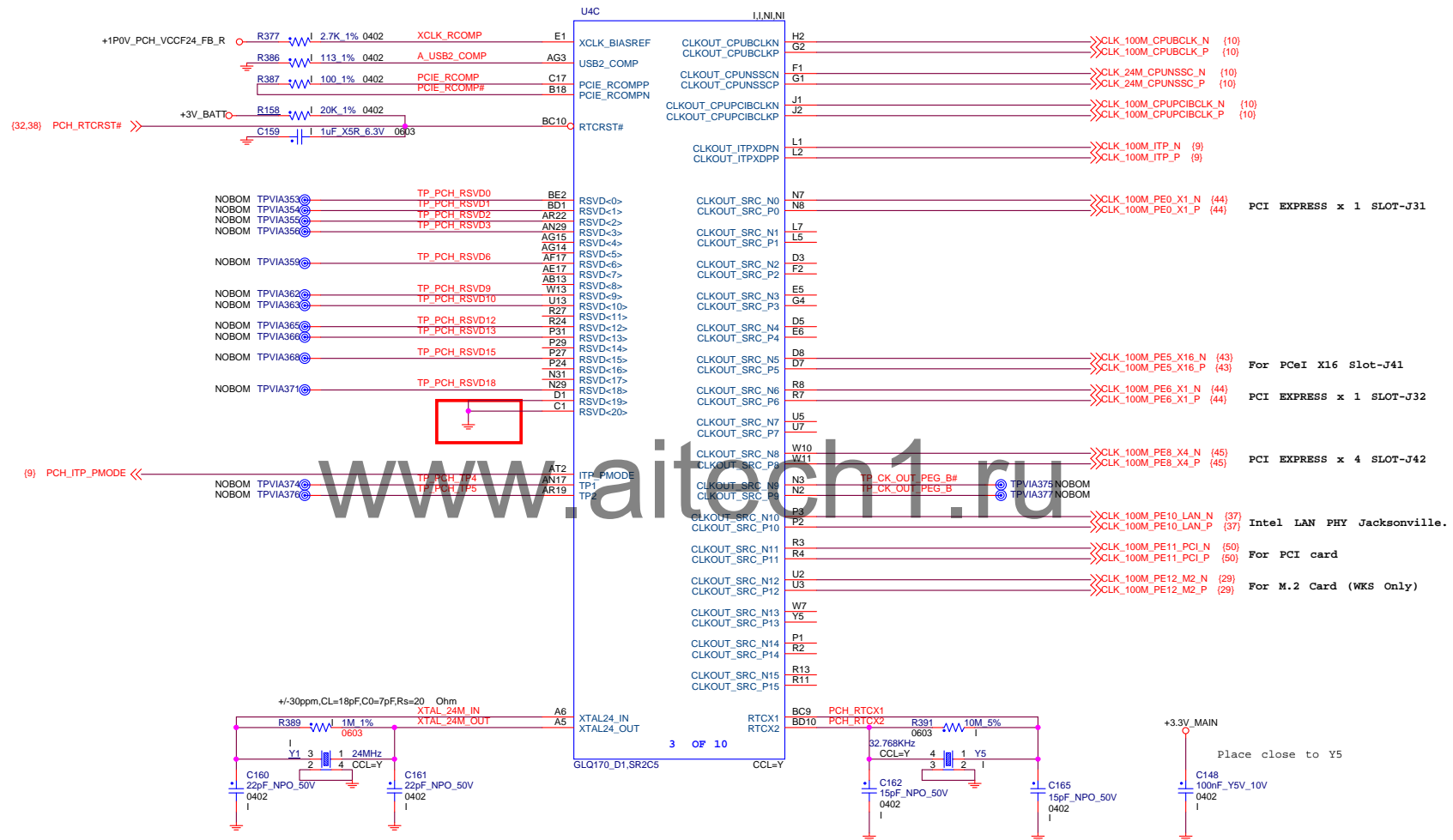
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Spitfire, Scorpion, Toledo, Z2
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Rev A	



PCH - CLOCK DISTRIBUTION

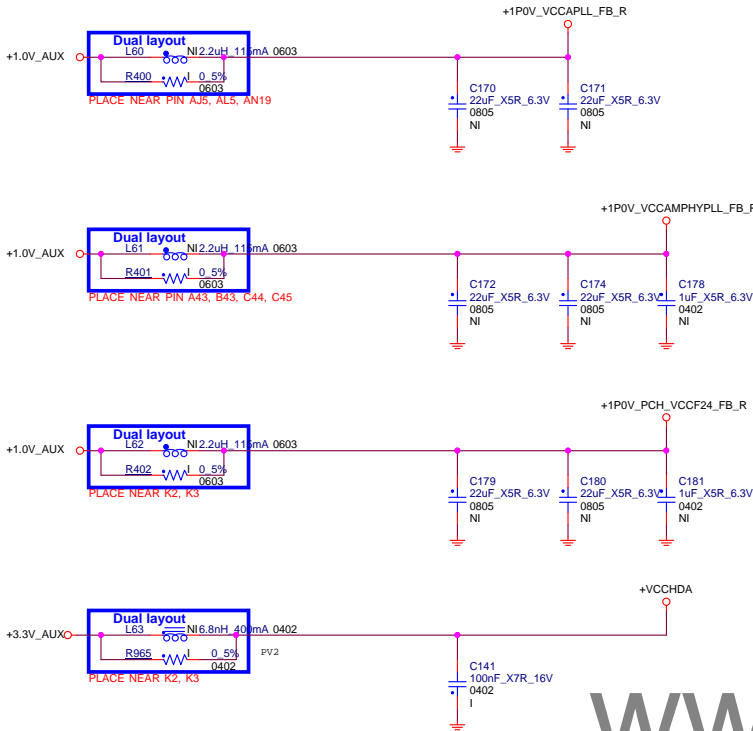


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Rev	A

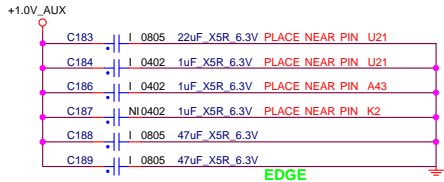
SKYLAKE Decoupling & filter

FILTER



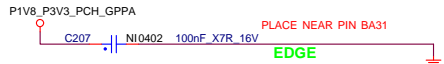
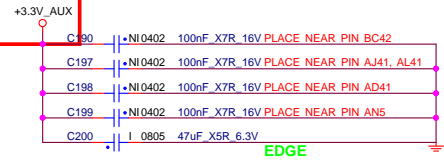
V1.0A

V3.3 DSW



V1.8A / V3.3A

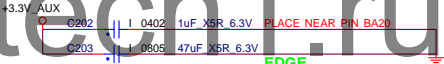
VccPGPPA



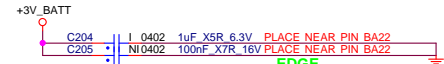
V1.8A / V1.8S / V3.3S



V3.3A



VCCRTC



Power Plane Isolation

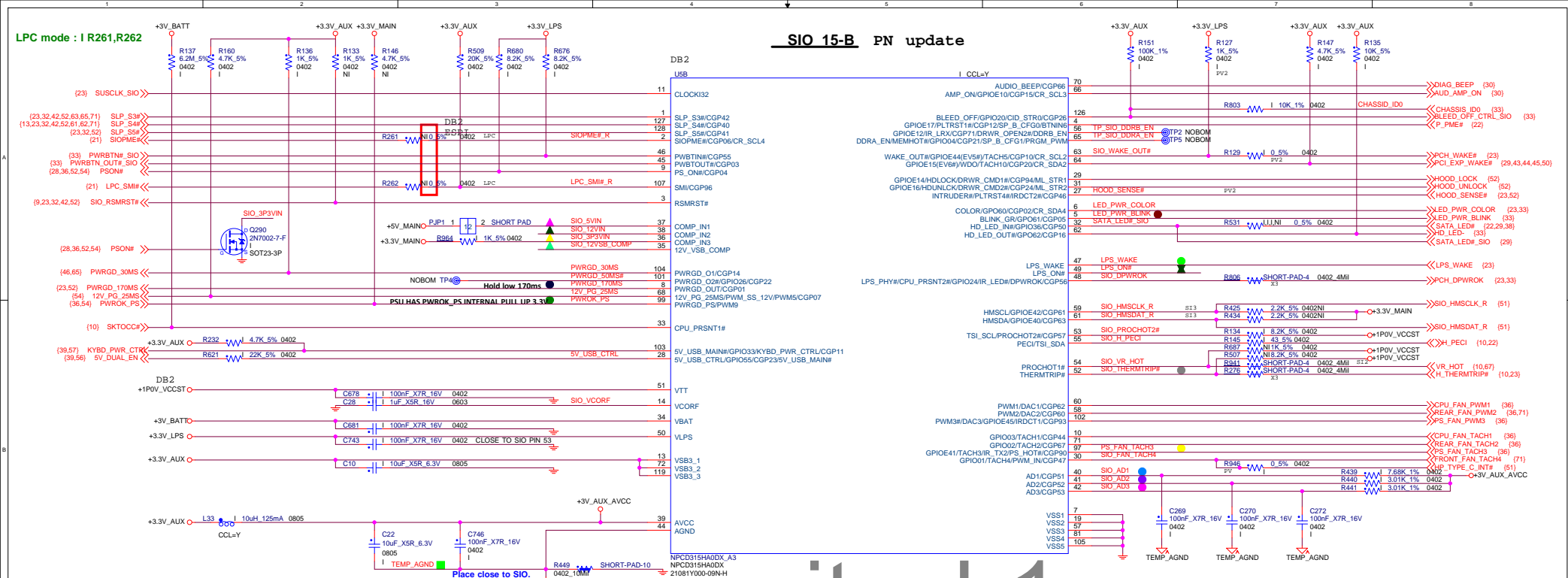
Need to update for SLK

Voltage	Interface	PCH Pins sharing power rail
VCC_PCH 1.05V	Core	U26, U25, U23, U21, V26,
	PCIe/SATA/ USB3	T19, T20, F22, P23, P25, F26, P28, P14, P16, P17
	GPIO/LPC	AC12
	FDI	M14
	DIFFCLK	U12, V14 W14 AB2
	SSC	T16, V16 AA16, W16
PCH 3.3V Standby	USB2	AF19, AF20, AF22, AF23, AP22
	SUS	AM33, AN33
	USB2	AH18, AH20, AH22, AJ20, AK20
	AZALIA	AW26
	RTC	AP35
PCH 3.3V	CLK	AM7, AM9, AP5, AP7, AR4, AT5, AV4, AW4, AW9, AG12, AK11,
	HVCMOS	AG1
	PCIe	AV3, AW3
	Fuse	U30, W30 AF26

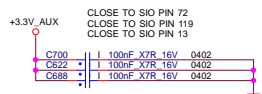
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Title PCH-PLL FILTER & DECOUPLING					
Size		Document Number		Rev	
Custom		795207-000		A	
Date: Monday, June 29, 2015		Sheet		26 of 72	

SIO 15-B PN update

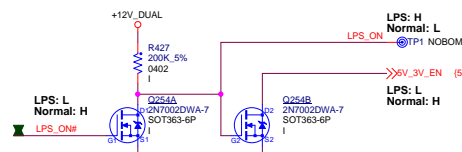


SIO15- SIO Input Power Decoupling Cap

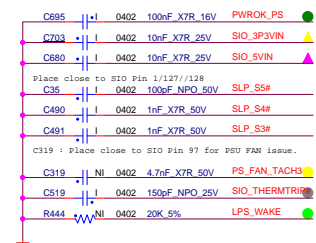


LPS_ON# / LPS_ON

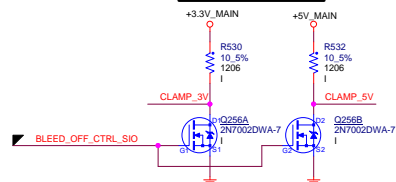
When LPS_ON# is asserted, the regular standby power rail is turned off and the small standby power well is activated.



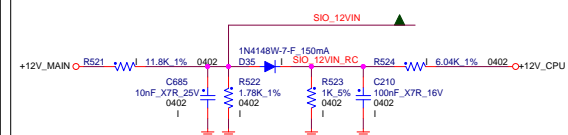
SIO15- SIO Critical Signal PU/PD + Decoupling



BLEED OFF 3.3V / 5V

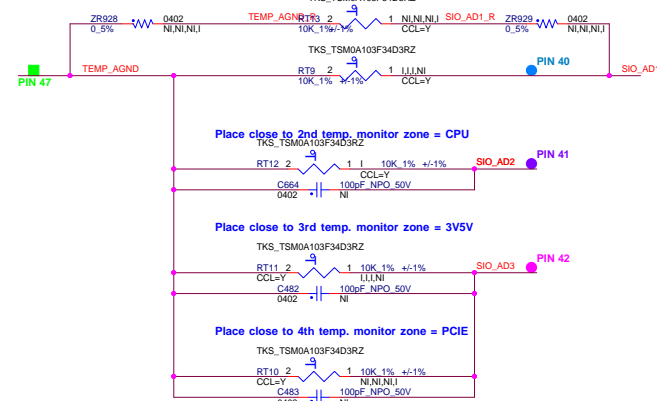


COMPARATOR INPUT 2 - 12V



THERMAL SENSORS (SIO15)

Place close to Ambient temp. monitor zone=Ambient

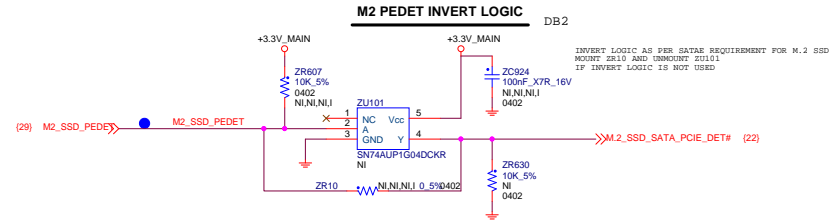
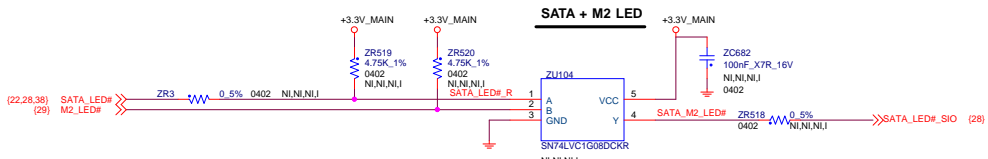
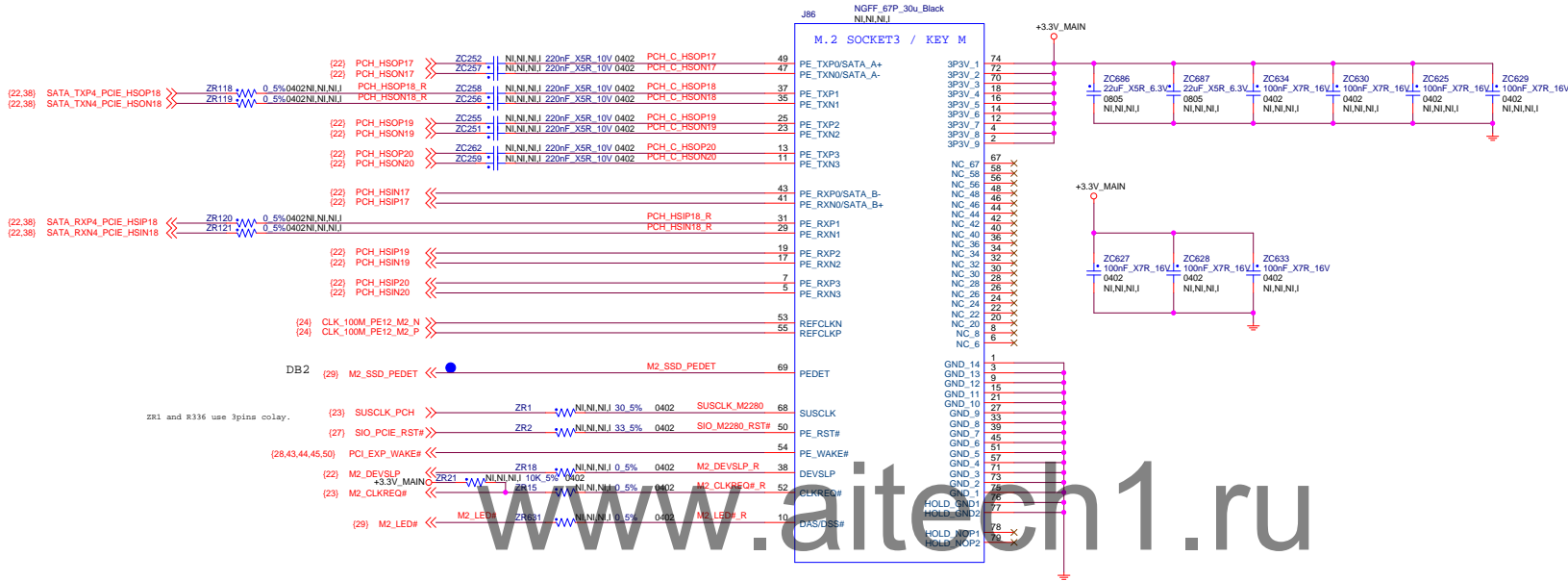


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WKS Only
M2. 2280 - STORAGE



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title	M2_SSD_SOCKET3(Z2 Only)
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Size	Document Number
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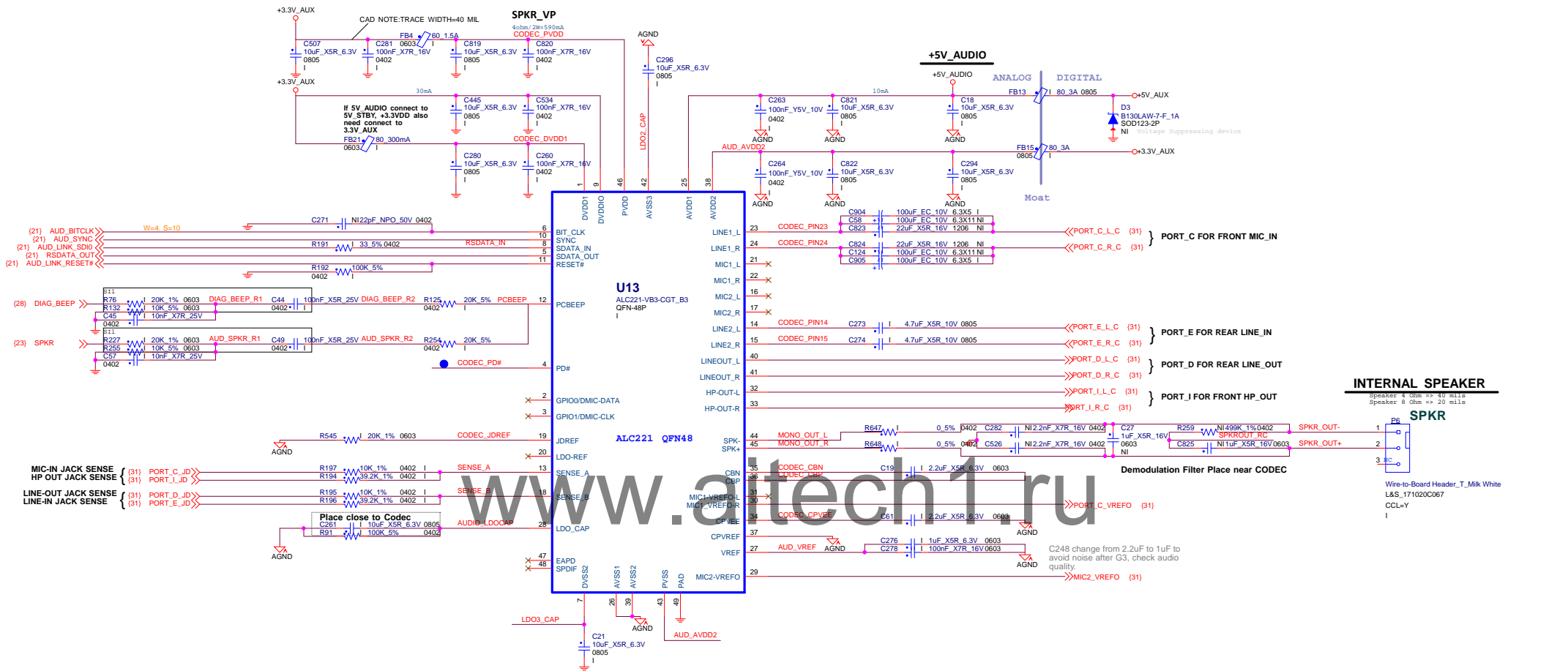
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Sheet	29	of	72
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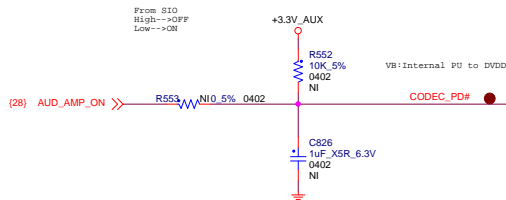
A

BOM DISTRIBUTION RULE
Spitfire, Scorpion, Toledo, Z2
(BOM,BOM,BOM, BOM)

HD AUDIO CODEC



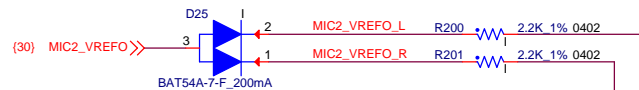
CODEC_PD# CONTROL CIRCUIT



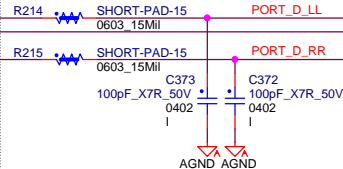
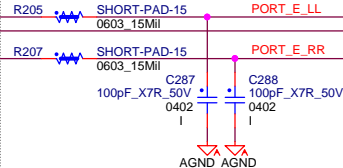
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Size Custom	Document Number 795207-000	Rev A	
Date: Monday, June 29, 2015	Sheet 30	of 72	

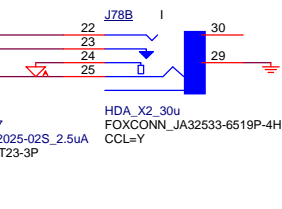


Close to connector →

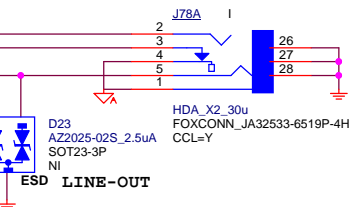


REAR AUDIO HEADER

PORT_E FOR REAR LINE_IN

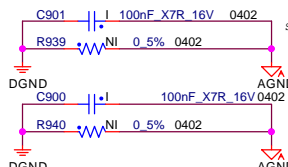
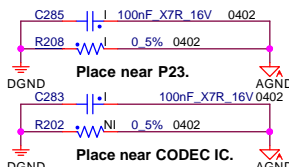
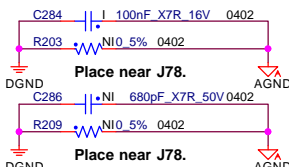
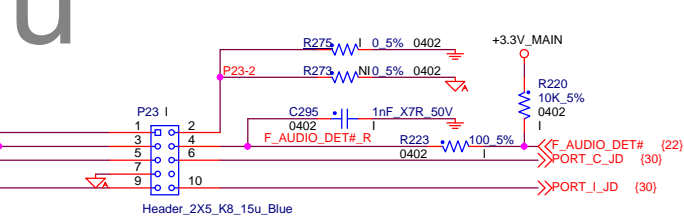
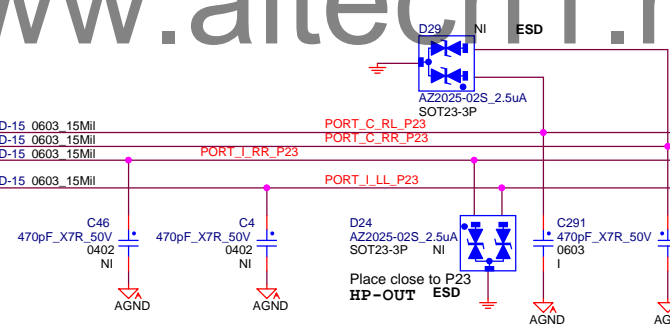
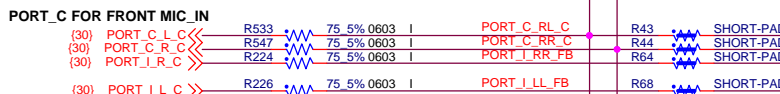
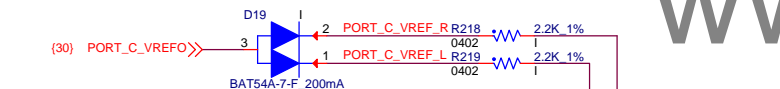


PORT_D FOR REAR LINE_OUT



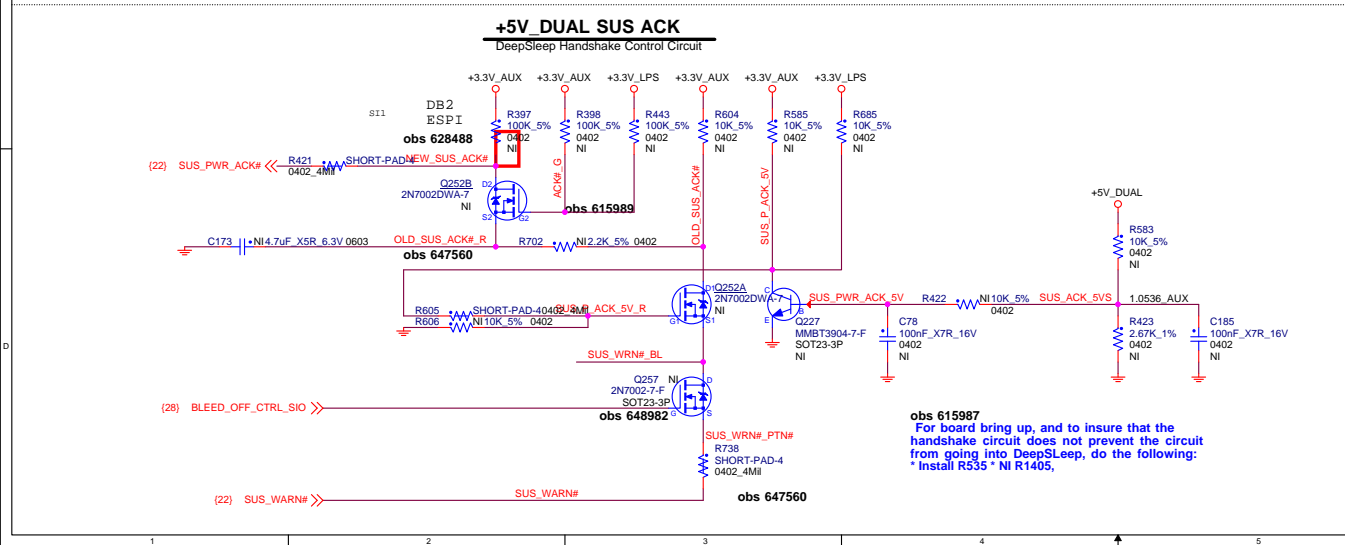
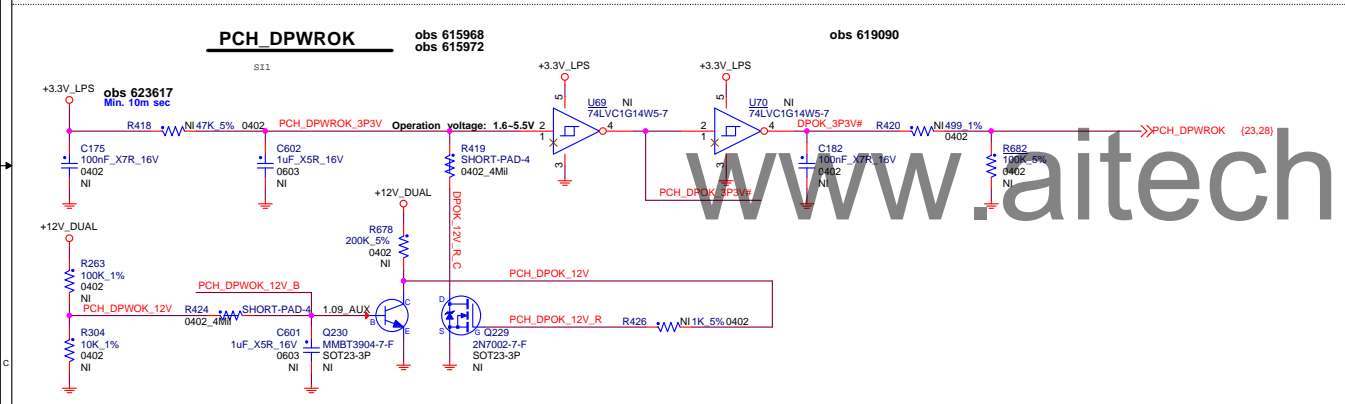
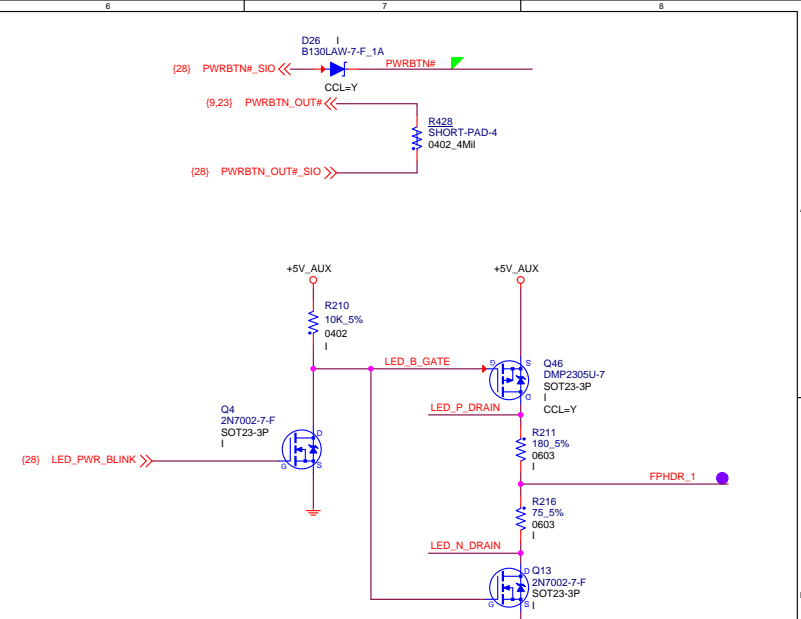
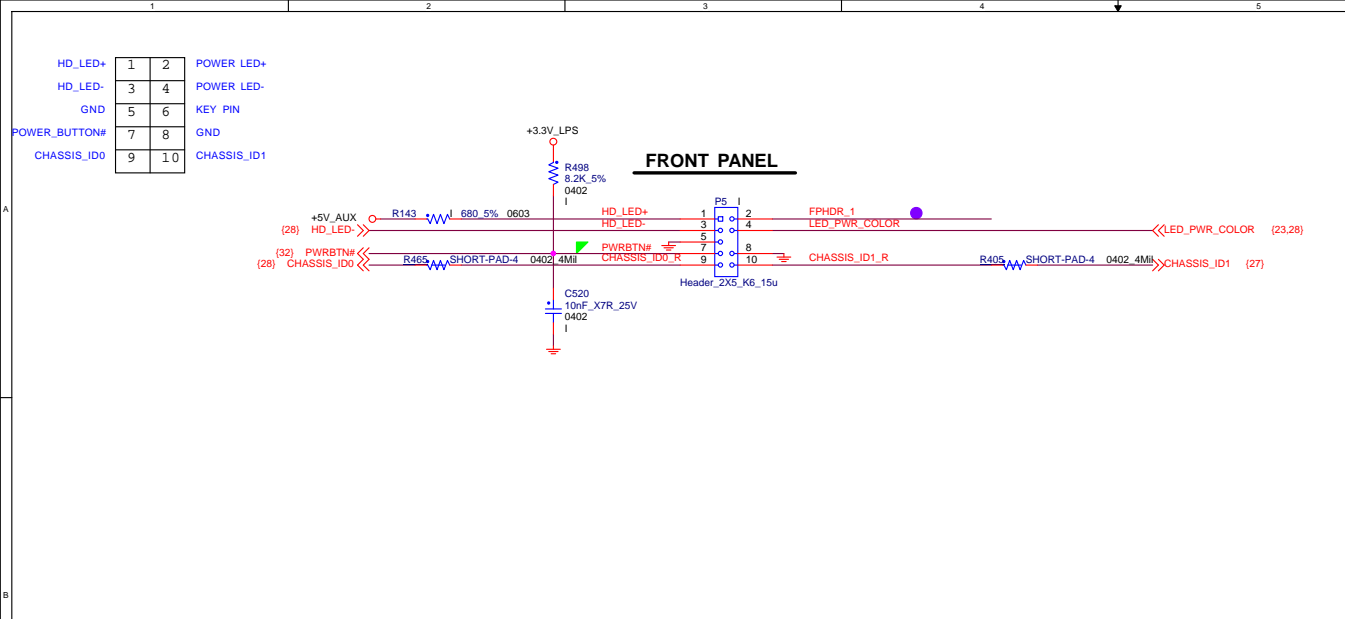
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FRONT AUDIO HEADER



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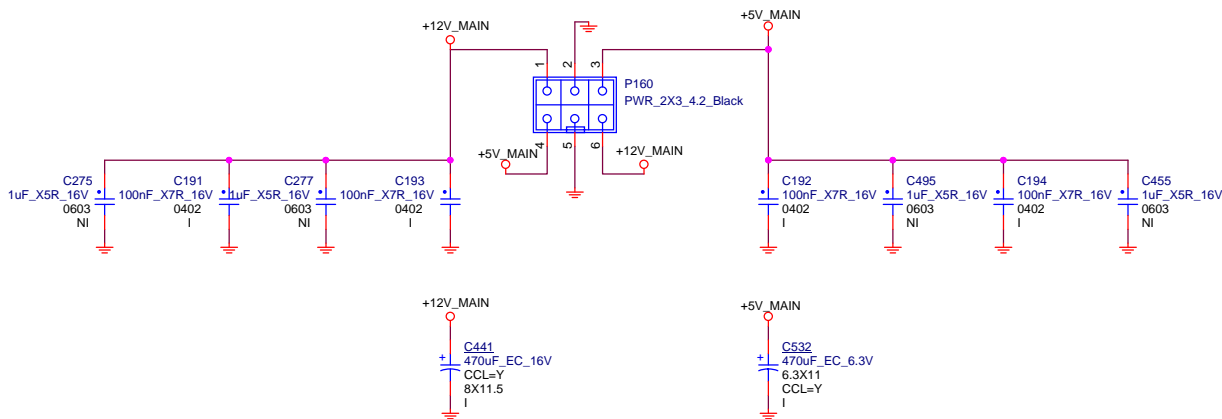
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Custom	795207-000	A	
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SATA POWER



PCB1

Printed Circuit Board

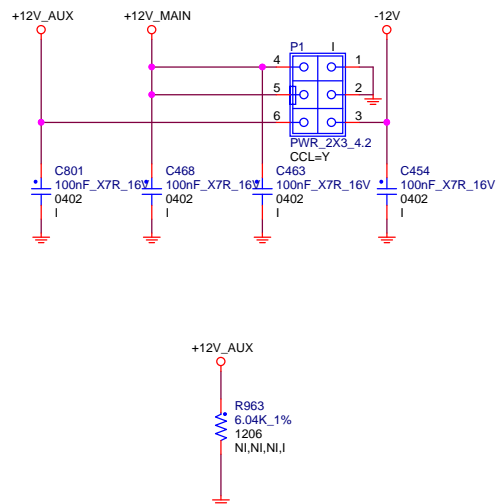
D800 PCB

PCB_REV:A

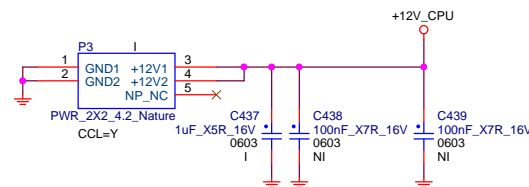
CCL=Y

4-Layer PCB, Color With Green Soldermask, White Silkscreen, NPG-TL, ML1, 9.6X9.6 inch, Rev:A, ROHS, HF 0101AQH08-35K-H

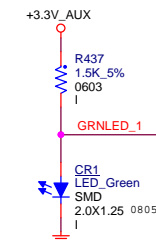
12V Power Connector




VR12V Power Input Connector



+3V_AUX LED

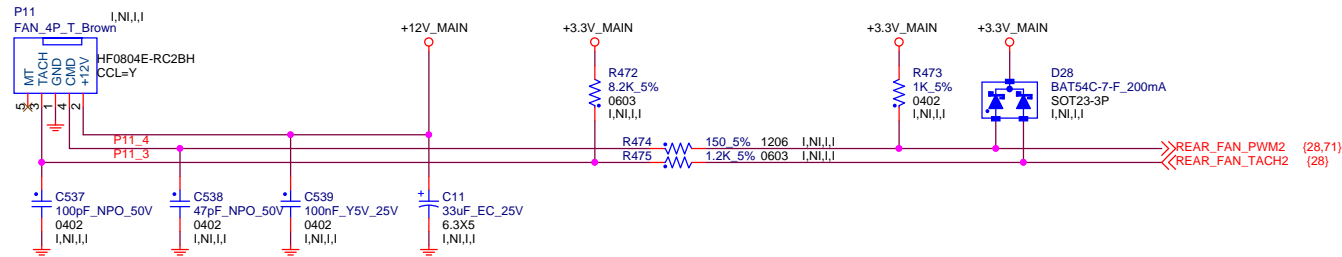


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PWR CON/AUXLED/PCB					
Size	Document Number			Rev	
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Rear Chasis FAN

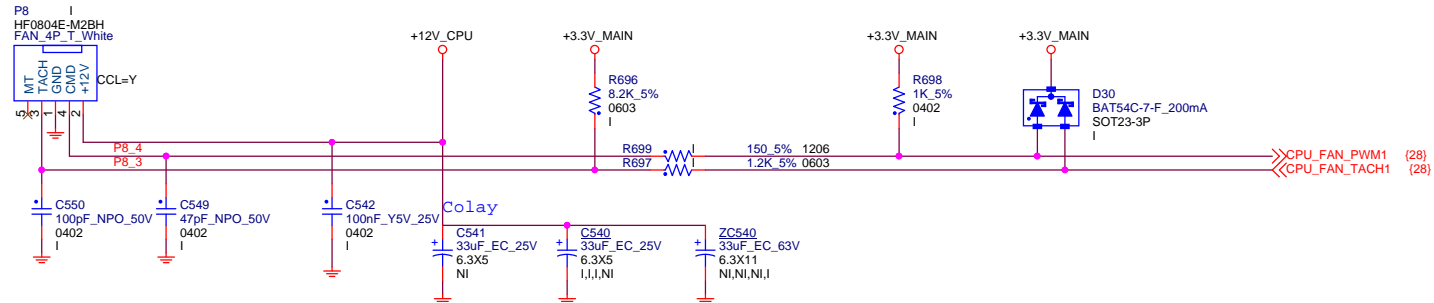
Color: Red



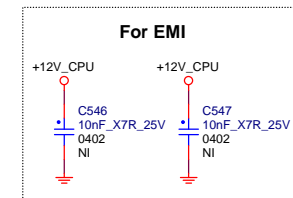
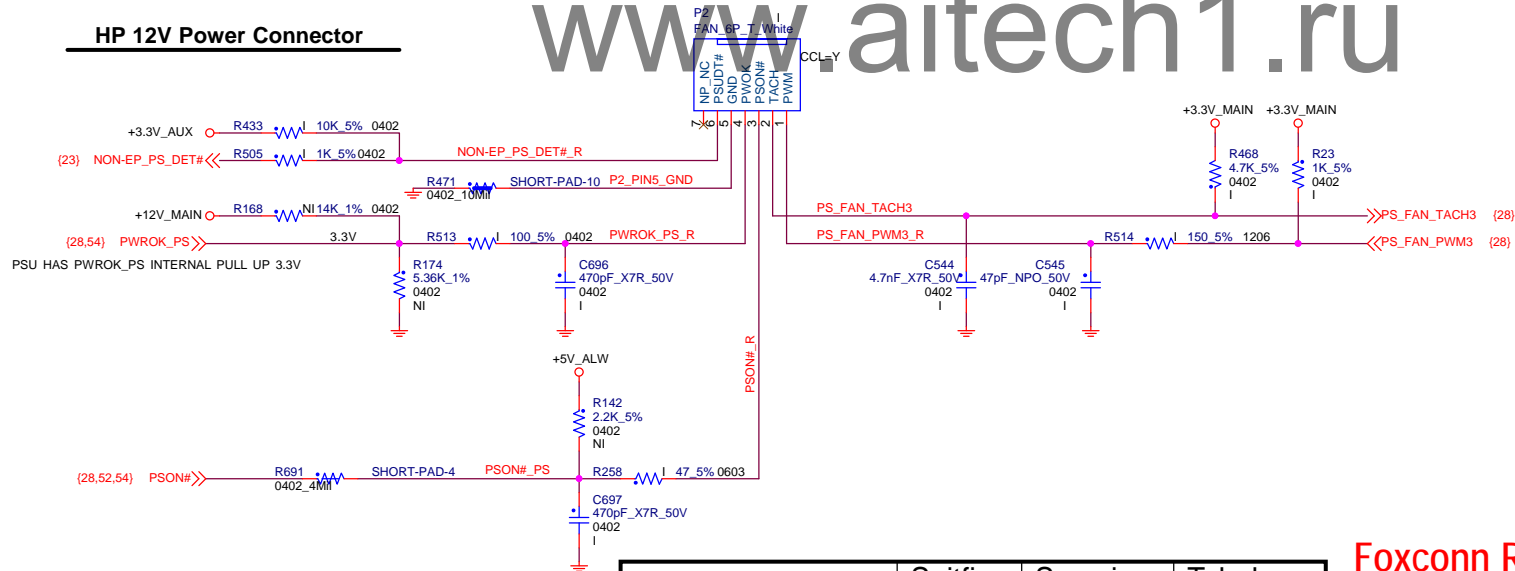
CPU FAN

Color: White

X3



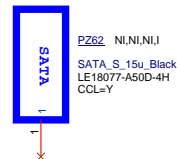
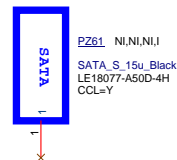
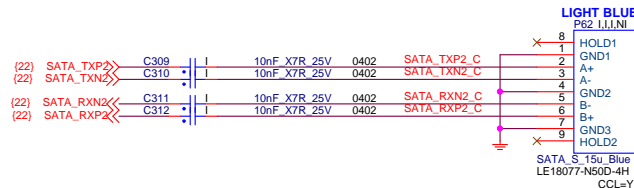
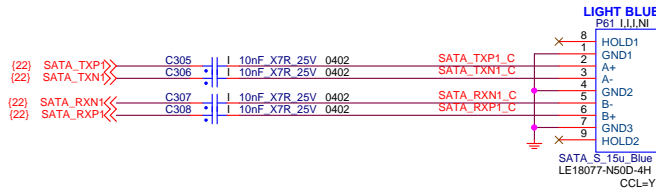
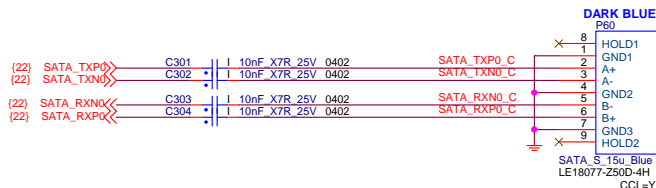
HP 12V Power Connector



	Spitfire	Scorpion	Toledo
CPU FAN - P8	1	1	1
Front FAN - P9	--	--	--
Rear FAN - P11	1	1	--
PSU FAN - P2	1	1	1

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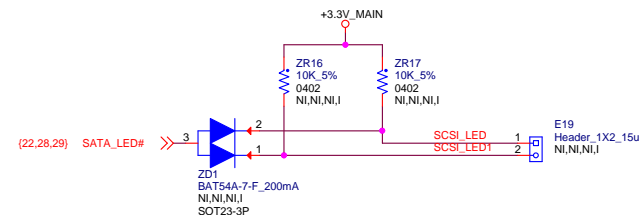
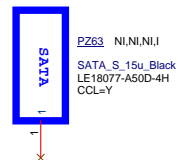
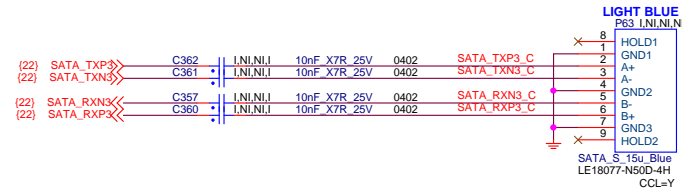
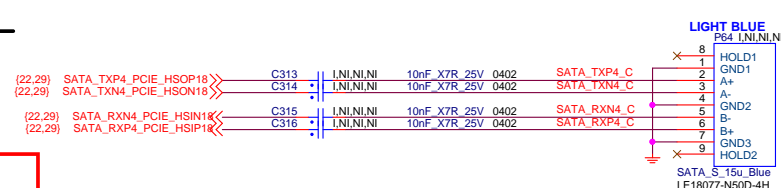
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Title FAN HEADERS/PSU PIN			
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SATA

Spitfire = 5 ports
Scorpion = 3 ports
Toledo = 3 ports
Bunun = 4 ports

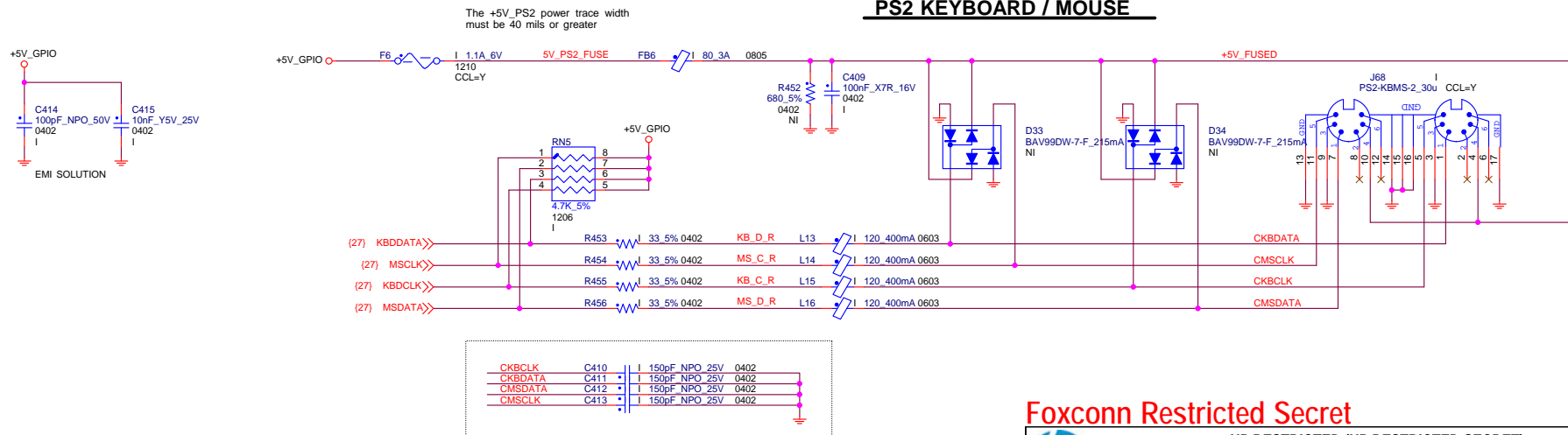
PCA spec doesn't
define the gold
plating.



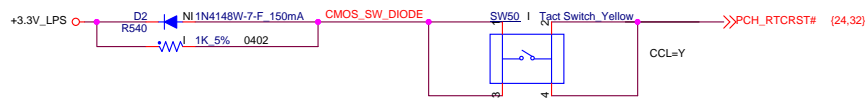
BOM DISTRIBUTION RULE
Spitfire, Scorpion, Toledo, Z2
(BOM,BOM,BOM, BOM)

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PS2 KEYBOARD / MOUSE



CLEAR CMOS BUTTON



CAD NOTE:
The PCB must have this
silkscreen for HPQ

This circuit disables the clear CMOS
function when system is powered



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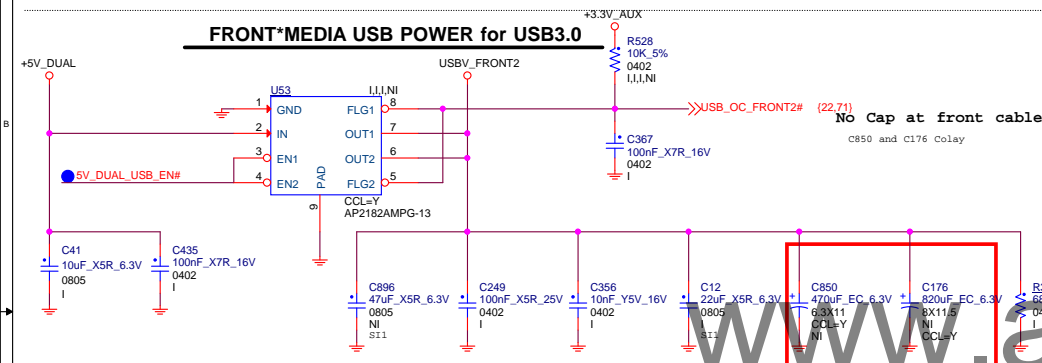
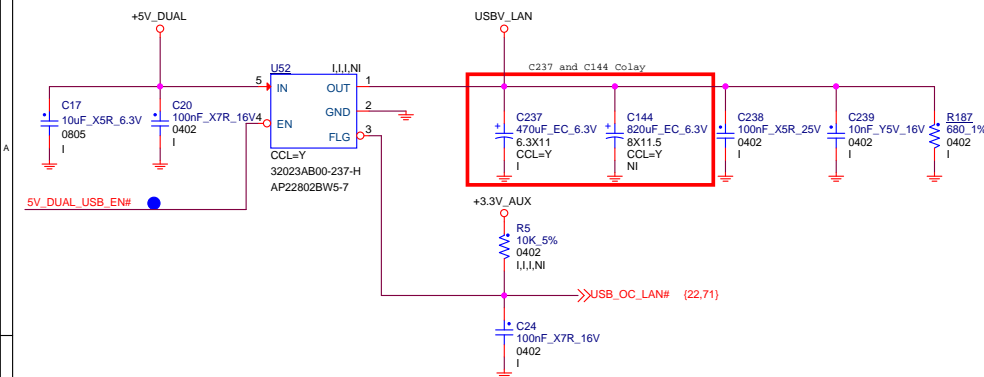
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Title **SATA/PS2/CMOS**

Size Document Number
Custom 795207-000

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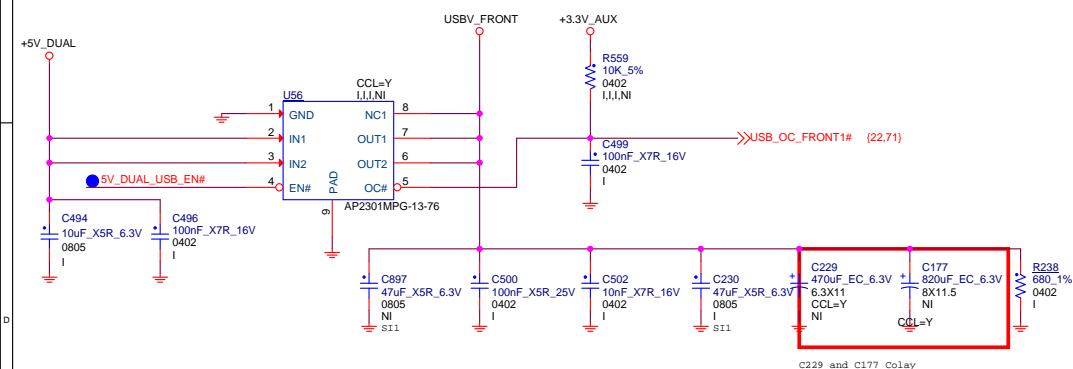
LAN+USB3x2



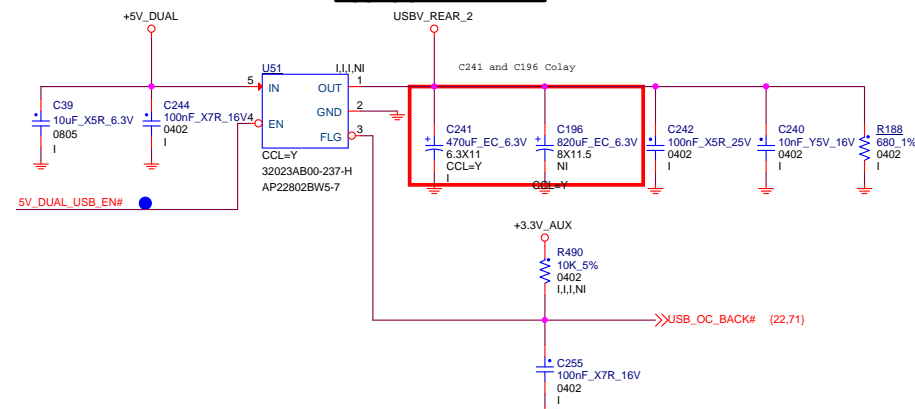
Have to check 2nd source's footprint and symbol

Combine the Front and Media power rail by one power switch topology. 1.5A/1CH - Dual CH

FRONT USB POWER for USB2.0

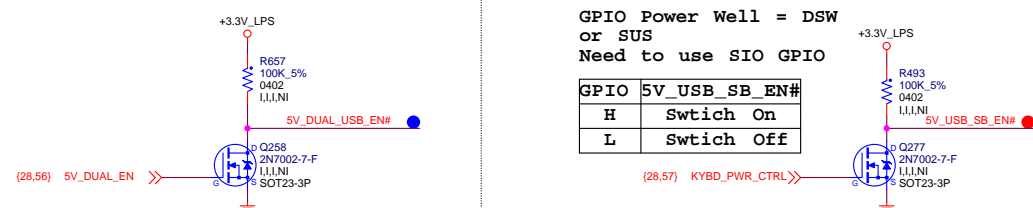
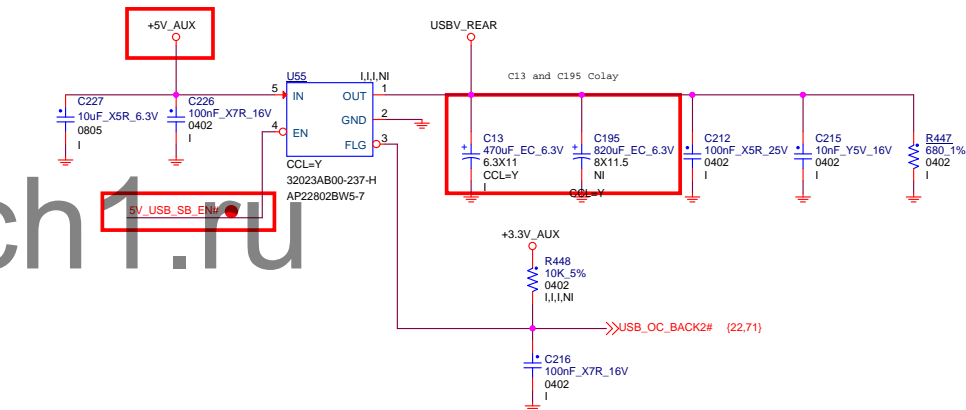


REAR USB POWER USB3.0x2



Wake-up event by USB device at S0-S5 state
2*USB3 Port
+5V_AUX + GPIO control

REAR USB POWER USB3.0x2



GPIO Power Well = DSW
or SUS
Need to use SIO GPIO

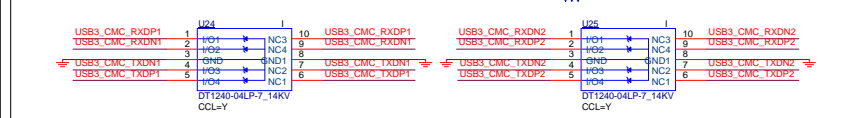
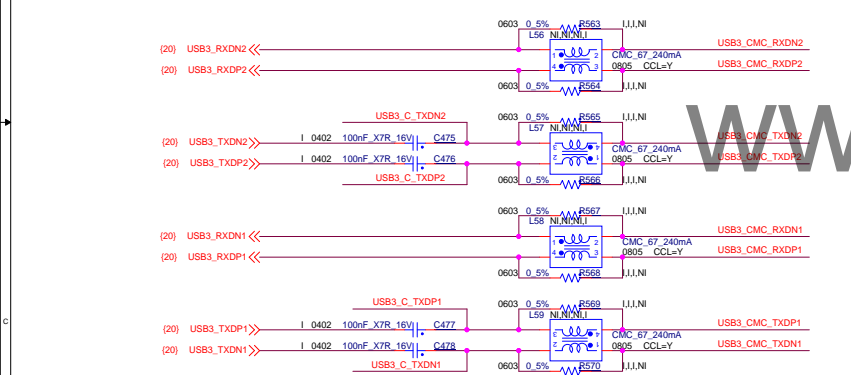
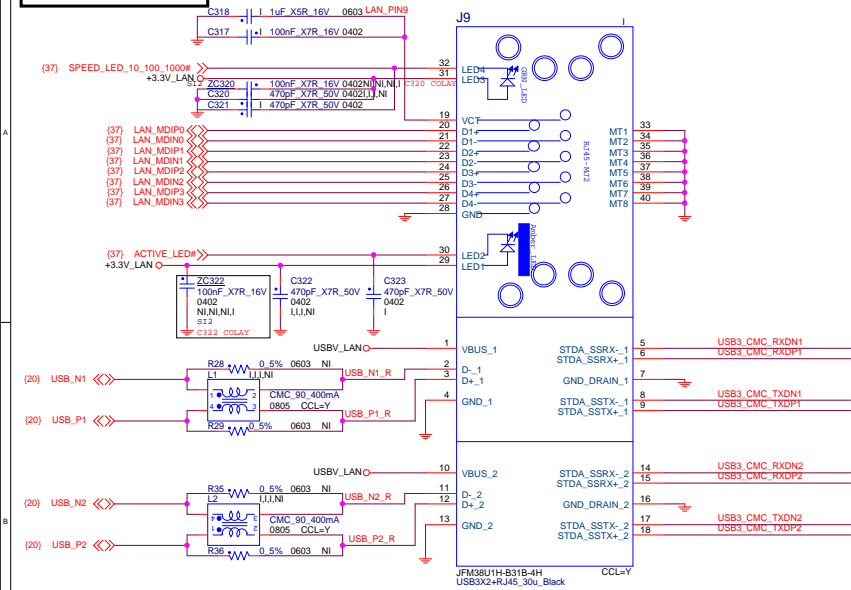
GPIO	5V_USB_SB_EN#
H	Switch On
L	Switch Off

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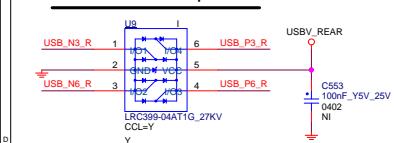
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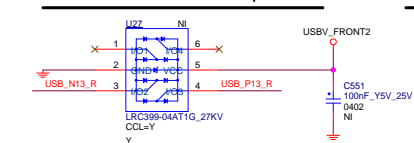
REAR LAN + USB



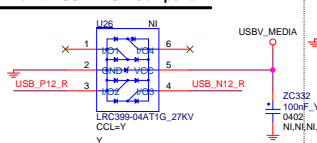
REAR USB ESD Component



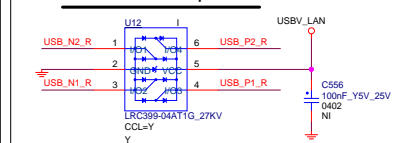
MEDIA READER USB ESD Component



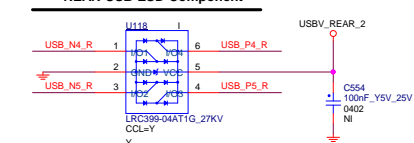
Internal USB2 ESD Component



LAN USB ESD Component



REAR USB ESD Component



BOM DISTRIBUTION RULE
Spitfire, Scorpion, Toledo, Z2

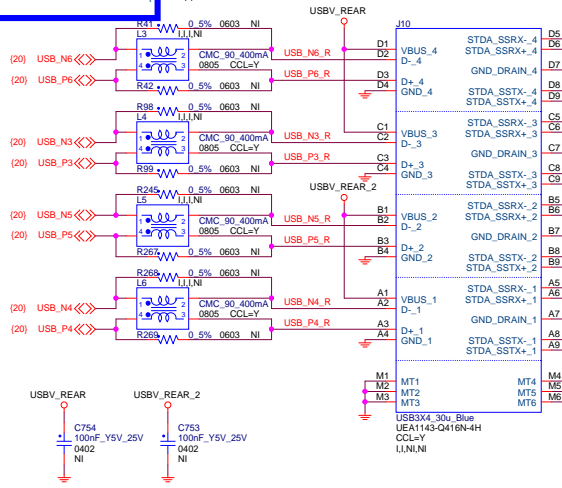
Toledo USB2+2 connector



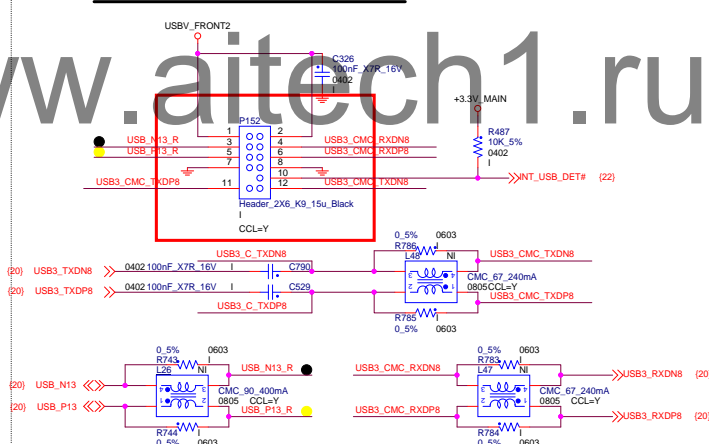
Bunun USB3*4 connector



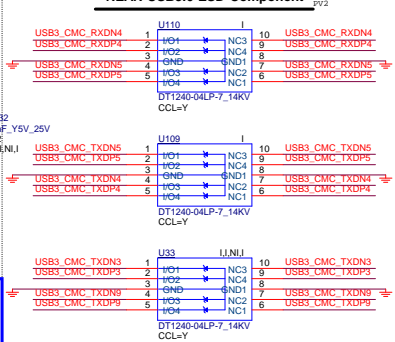
0.9 A PER PORT



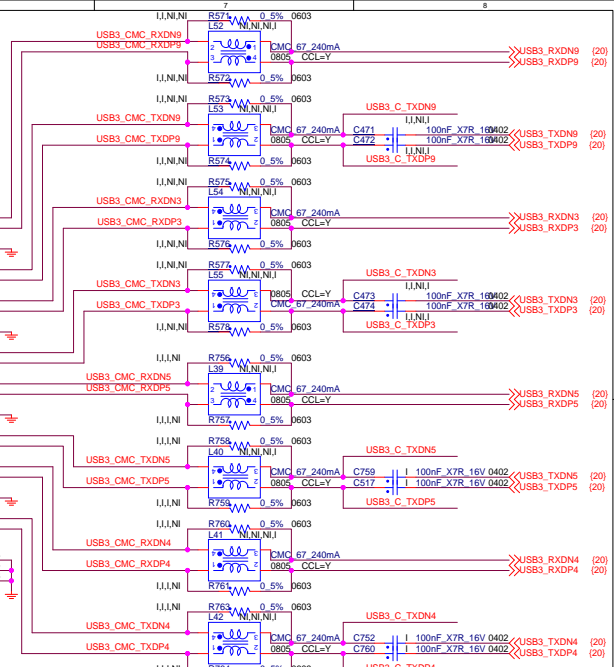
MEDIA2 READER USB HEADER



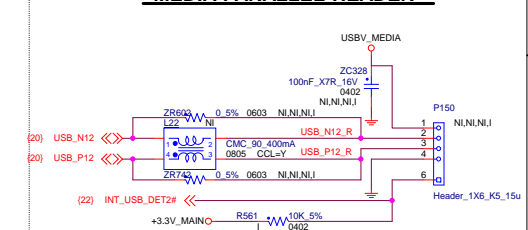
REAR USB3.0 ESD Component SI3



REAR USB 3.0



MEDIA PARALLEL HEADER



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Title	REAR/RJ45/MEDIA USE
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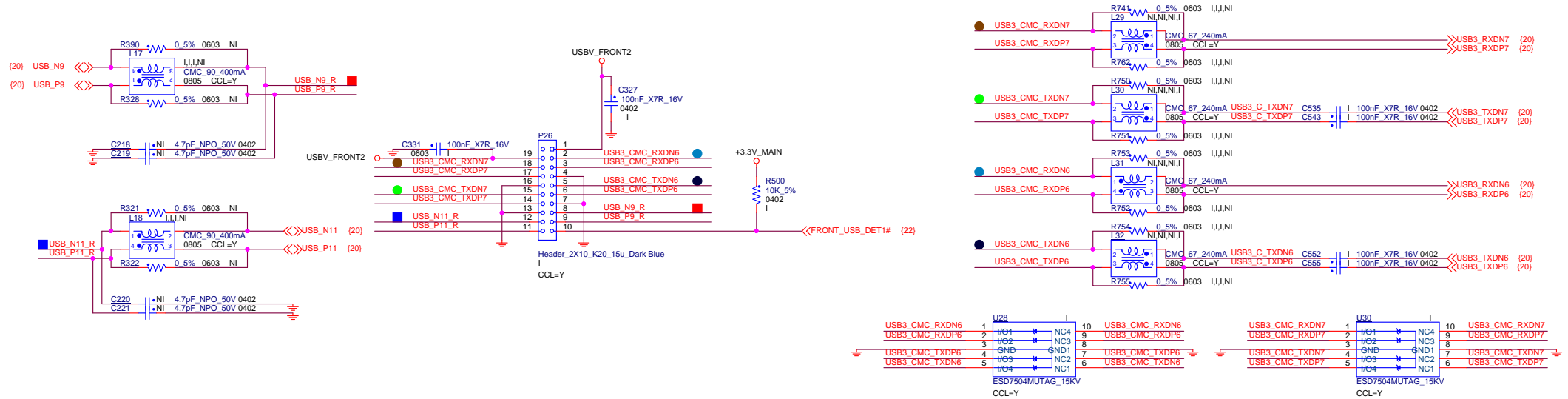
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C	795207-000
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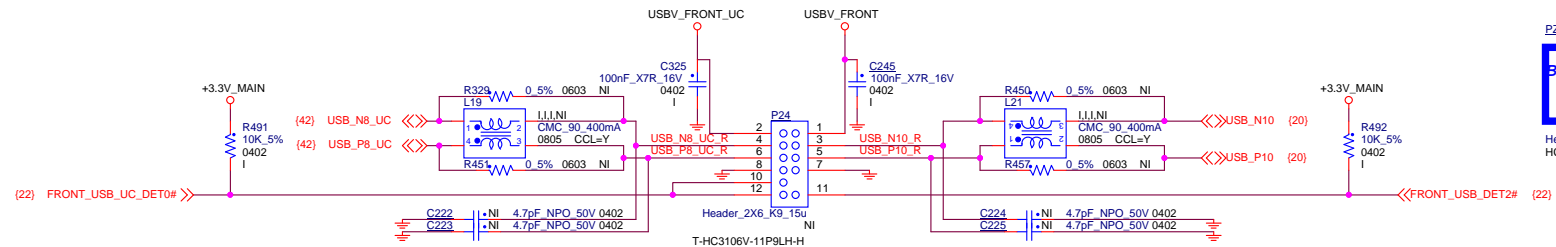
2

FRONT2 USB 3.0 HEADER



FRONT1 USB 2.0 HEADER

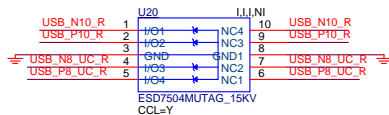
Only One USB2.0 port support Charging.
The power rail have to be seperated



1. Need to change to 2x6 with key9&10
2. Need to support Charging port
3. PN = HC3106V-1YP2LH (HIGH TEMP)
4. PN = JC1106V-YP2BH (PA66)

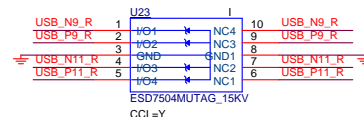
BOM DISTRIBUTION RULE
Spittfire, Scorpion, Toledo, Z2
(BOM,BOM,BOM, BOM)

FRONT2 USB ESD Component



FRONT2 USB ESD Component

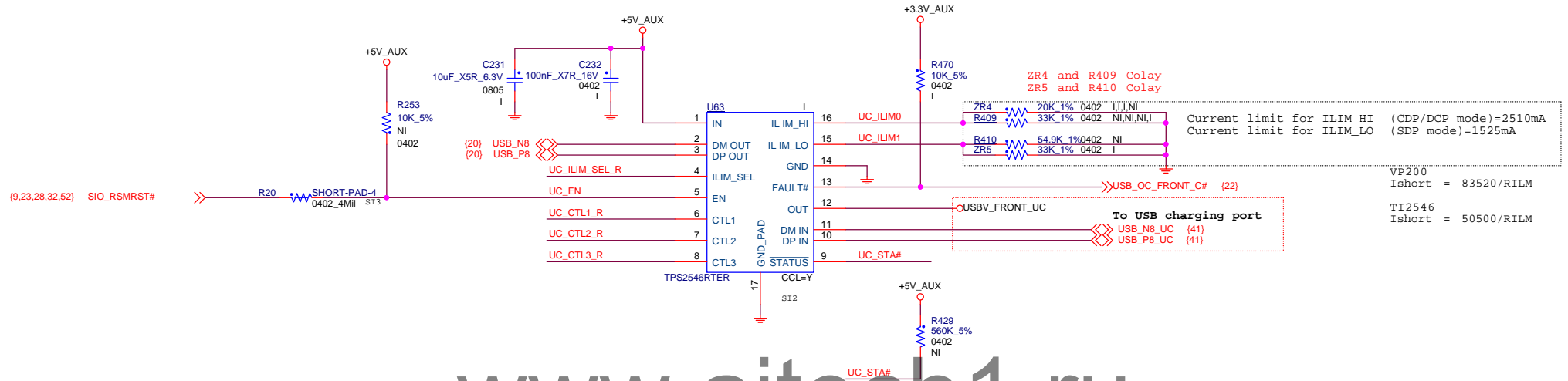
FRONT1 USB ESD Component



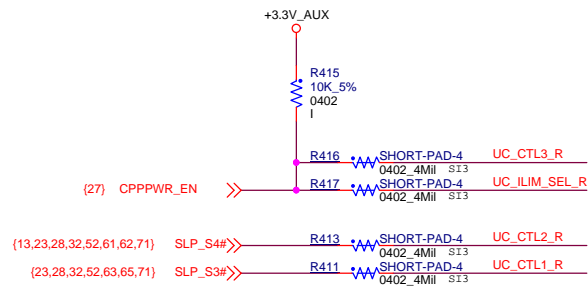
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Title FRONT USB/HEADER	
Size Document Number	Rev
Custom 795207-000	A
Date: Monday, June 29, 2015	Sheet 41 of 72

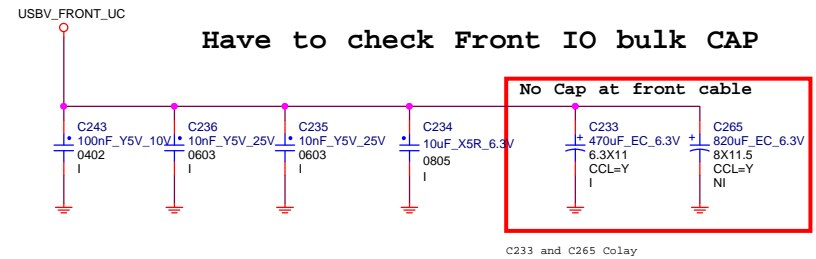
USB CHARGER



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PCH GPIO41 for PCH_CHAR_CTL3
(H-->CDP, L-->SDP)



USB Charging mode selection in System Status

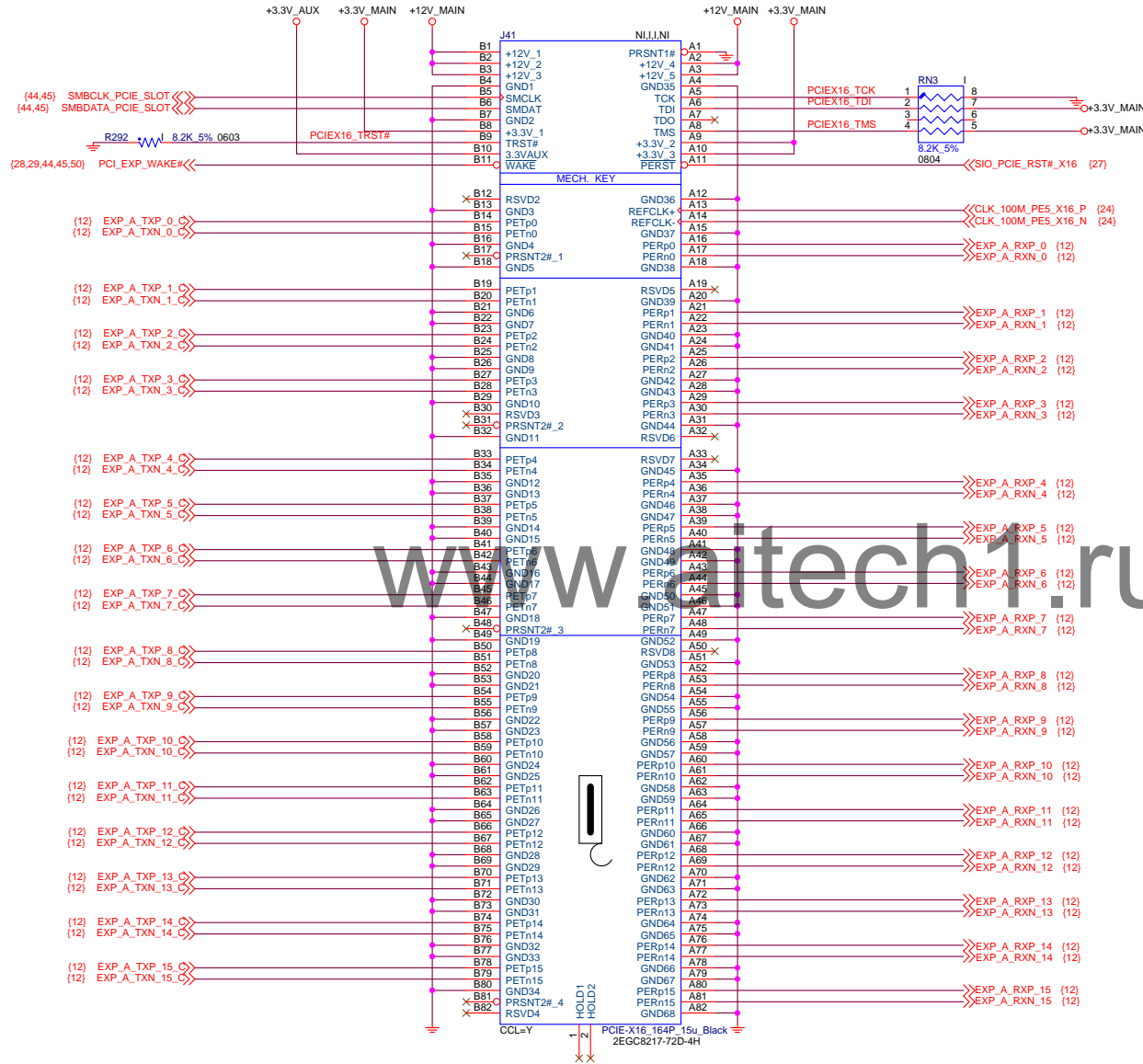
State	bit	CTL1 SLP_S3#	CTL2 SLP_S4#	CTL3 CPPPWR_EN	ILIM_SEL	Mode	ILIM
S0		1	1	1	1	CDP	ILIM = 2510mA
S0		1	1	0	0	SDP	ILIM = 1525mA
S3		0	1	1	1	DCP_AUTO	ILIM = 2510mA
S3		0	1	0	0	SDP	ILIM = 1525mA
S4/S5		0	0	1	1	DCP	ILIM = 2510mA
S4/S5		0	0	0	0	TURN OFF SWITCH	ILIM = 1525mA

BOM DISTRIBUTION RULE
Spitfire, Scorpion, Toledo, Z2
(BOM,BOM,BOM, BOM)

Foxconn Restricted Secret

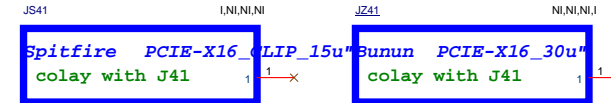
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Title USB CHARGER					
Size	Document Number	Rev A			
Custom	795207-000				
Date:	Monday, June 29, 2015	Sheet	42	of	72

PCI EXPRESS x16 SLOT



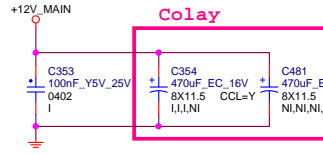
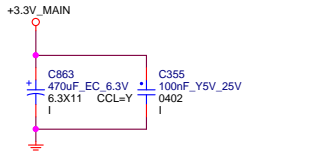
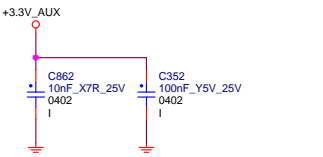
www.mitech1.ru

Need to change to 15u" for ENT
2EG78217-72DL-4H



Spitfire PCIE-X16_15u" CLIP 15u" colay with J41

Bunun PCIE-X16_30u" colay with J41

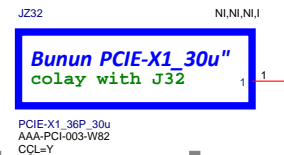
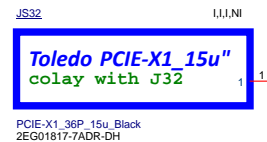
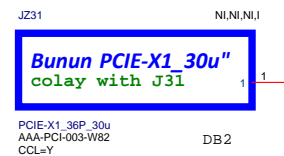
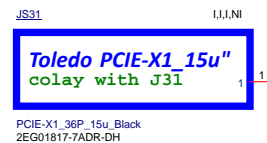
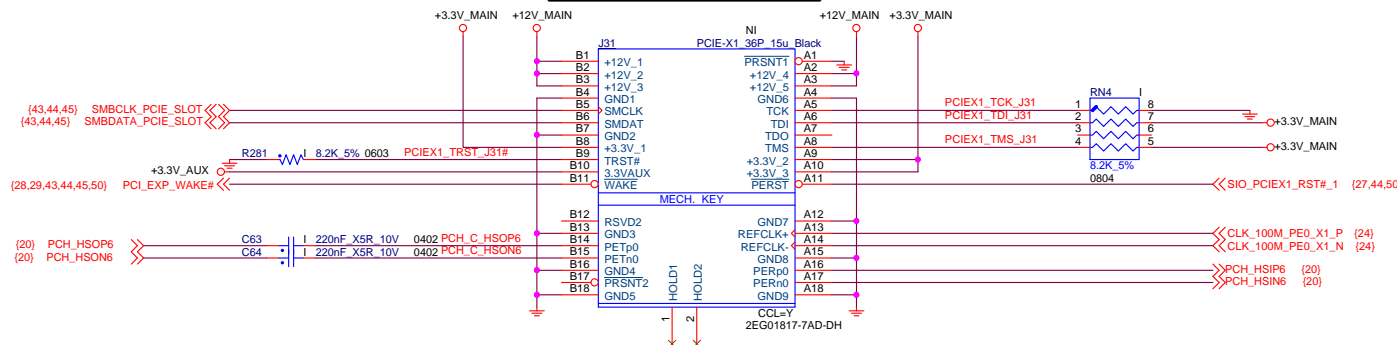


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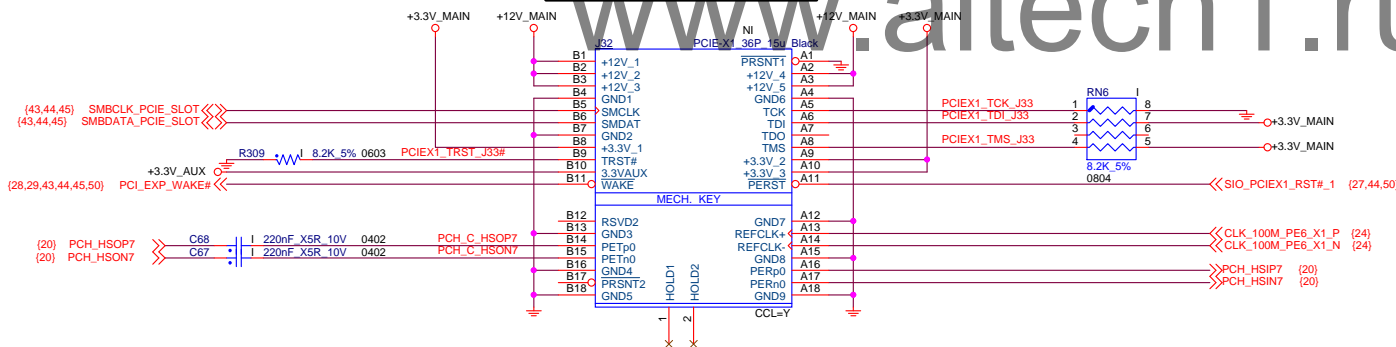
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Title PCIE - x16			
Size	Document Number	Rev	
Custom	795207-000	A	
Date:	Monday, June 29, 2015	Sheet	43 of 72

Z2 leverage change item

PCI EXPRESS X1 SLOT1



PCI EXPRESS X1 SLOT1

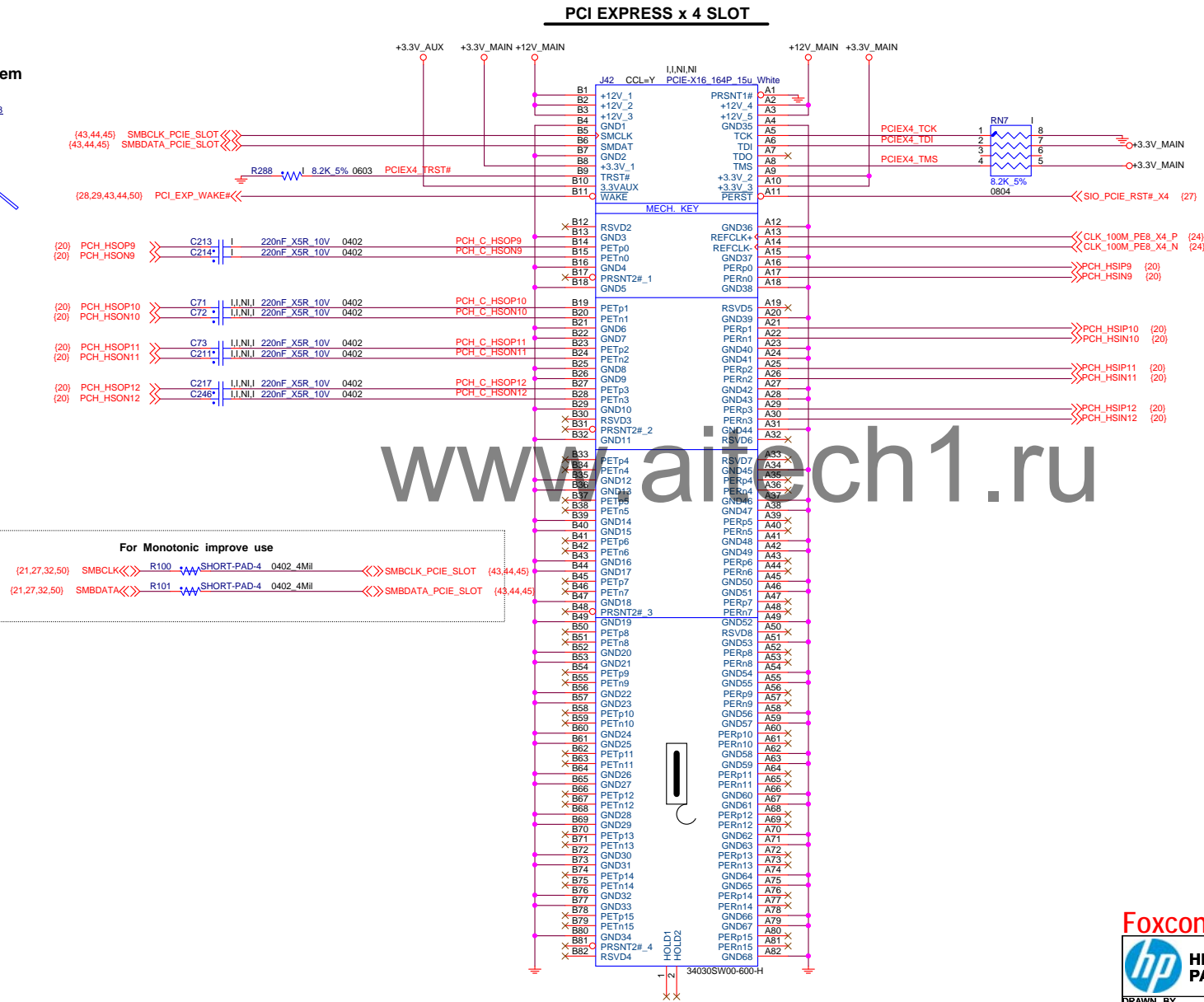
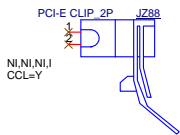


	SIO_GPIO25	SIO_GP60 / CLAMP_CTRL	+3_3V_SLOT
S0	X	L	ENABLE
S3 / S5	H	H	ENABLE
WOL DISABLE	L	H	DISABLE

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Title PCIE - x1			
Size	Document Number	Rev	
Custom	795207-000	A	
Date:	Monday, June 29, 2015	Sheet	44 of 72

Z2 leverage change item

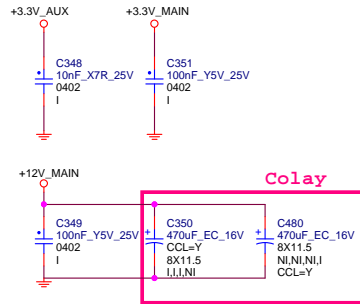


Toledo PCIE-X1_15u"
colay with J42

PCIE-X1_36P_15u_Black
2EG01817-7ADR-DH

Bunun PCIE-X16_30u"
colay with J42

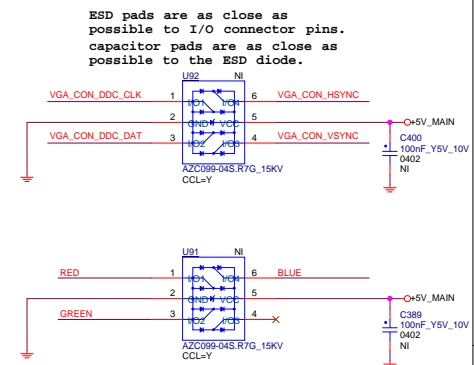
PCIE-X16_164P_30u
2EG08213-72D-DH
CCL=Y



BOM DISTRIBUTION RULE
Spitfire, Scorpion, Toledo, Z2
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Size	Document Number
3	7000000-000

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Sheet	46	of	72

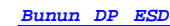
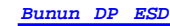
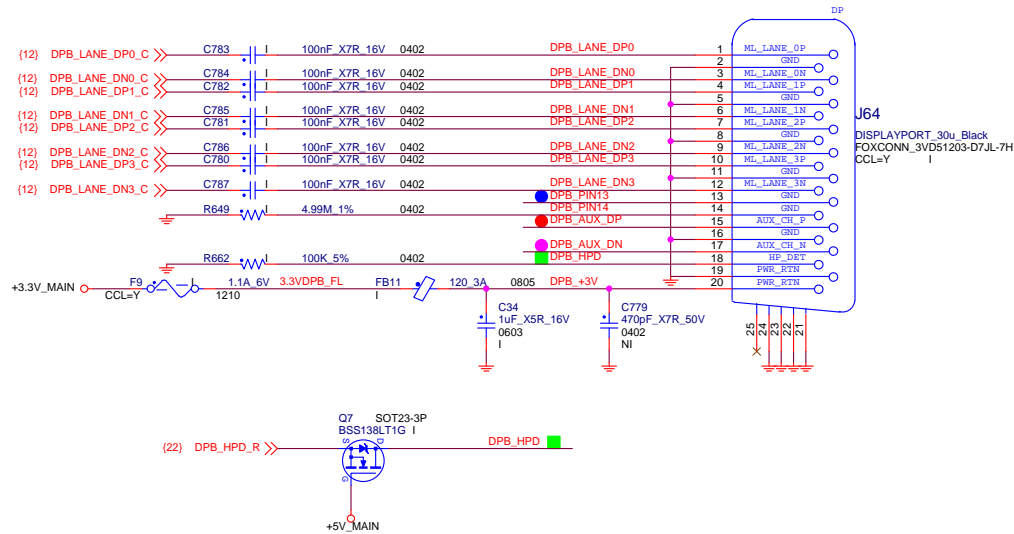
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RS232_9P_20u_Teal
DM10192-H543-4H
CCL=Y

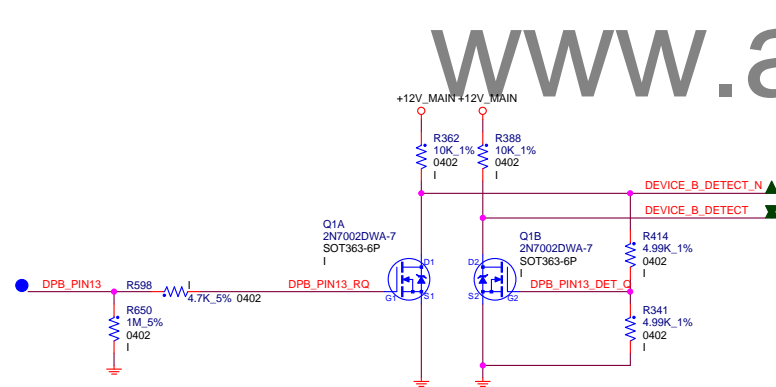
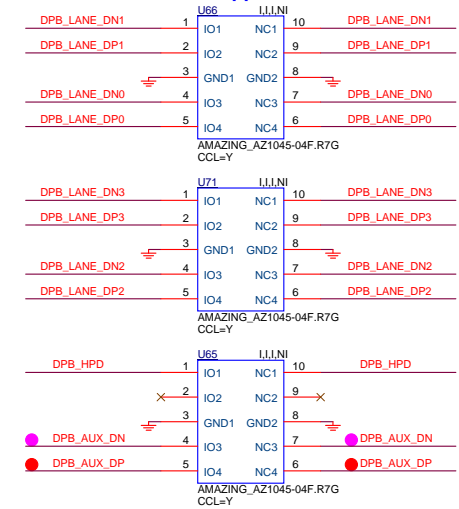
JZC

3

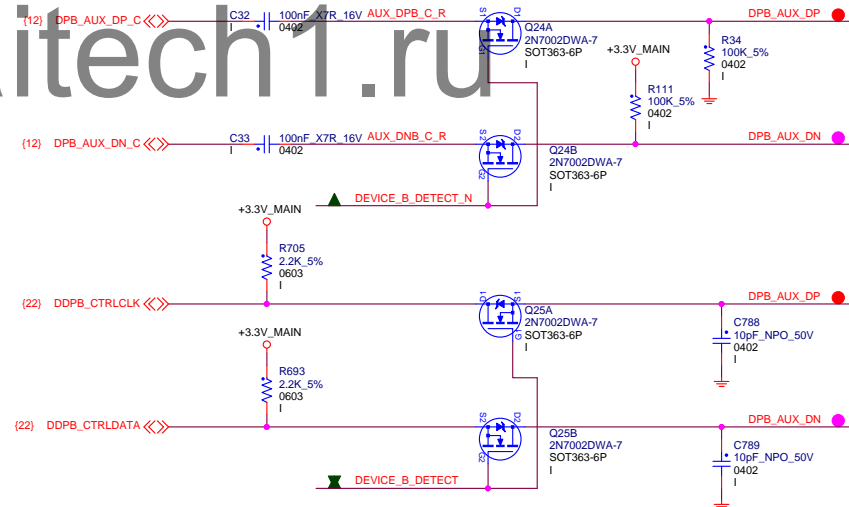
DISPLAY PORT



ESD suppressor



PIN13		FUNCTION
DP	DONGLE	
L	X	DEVICE_C_DETECT
X	H	DEVICE_C_DETECT_N



BOM DISTRIBUTION RULE
Spittfire, Scorpion, Toledo, Mondial
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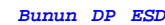
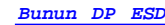
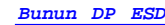
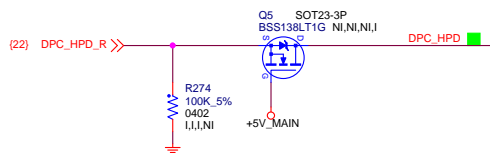
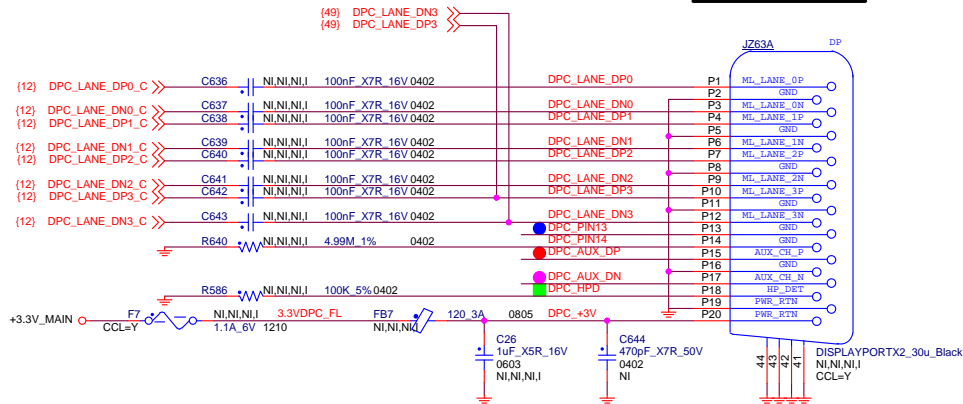
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Size	Document Number
Custom	795207-000

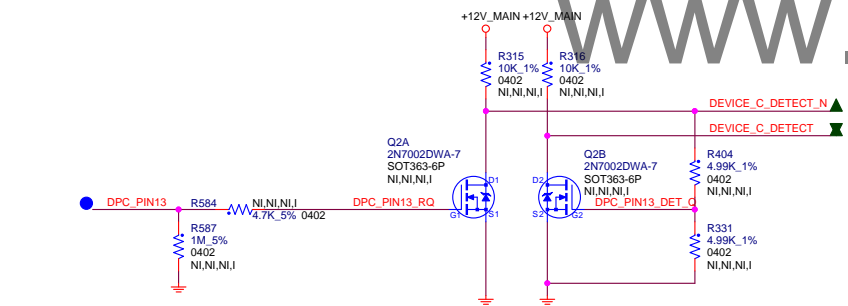
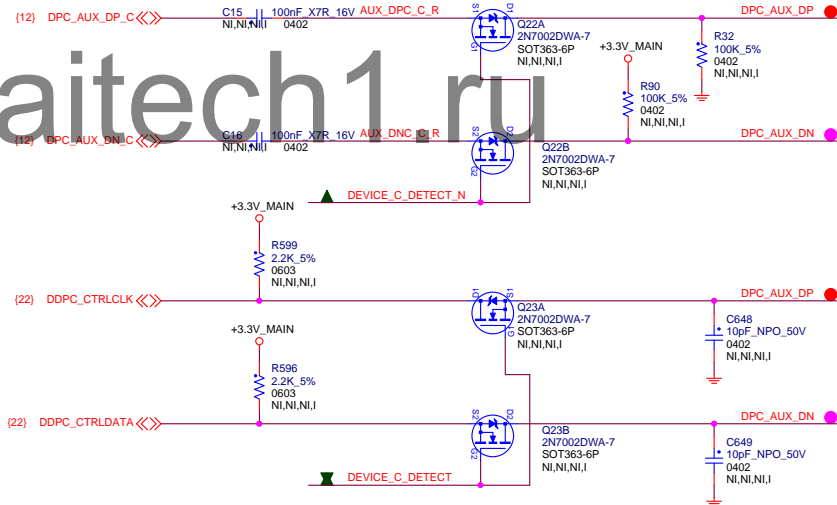
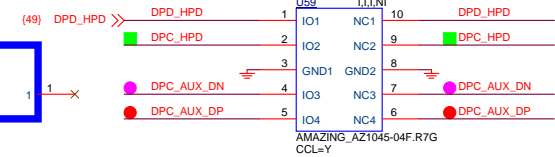
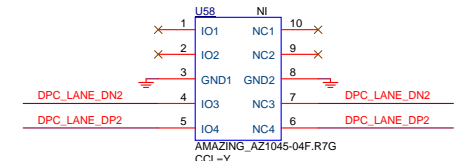
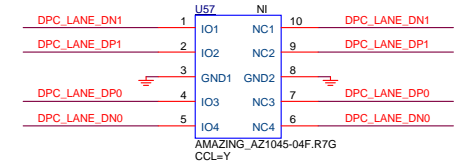
Date: Monday, June 29, 2015

Rev
A

WKS Only
DISPLAY PORT



ESD suppressor



PIN13		FUNCTION
DP	DONGLE	
L	X	DEVICE_C_DETECT
X	H	DEVICE_C_DETECT_N

BOM DISTRIBUTION RULE
Spitfire, Scorpion, Toledo, Z2
(BOM,BOM,BOM, BOM)

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Title	DISPLAY PORT 2(DUAL-C)
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Size	Document Number
Custom	795207-000

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Rev
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A	
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DISPLAYPORT_30u_Black
3VD11203-3D71-4H
CCL=Y
34044FA00-600-H

Bunun DP ESD

DISPLAY PORT

Bunun DP ESD



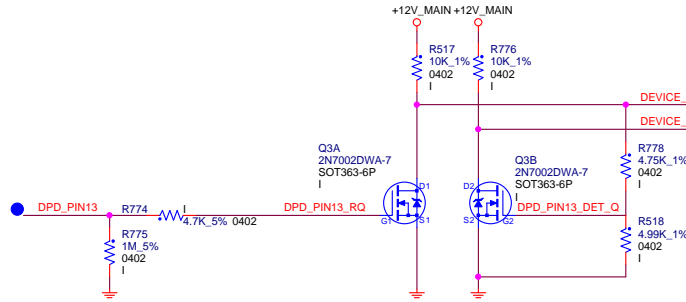
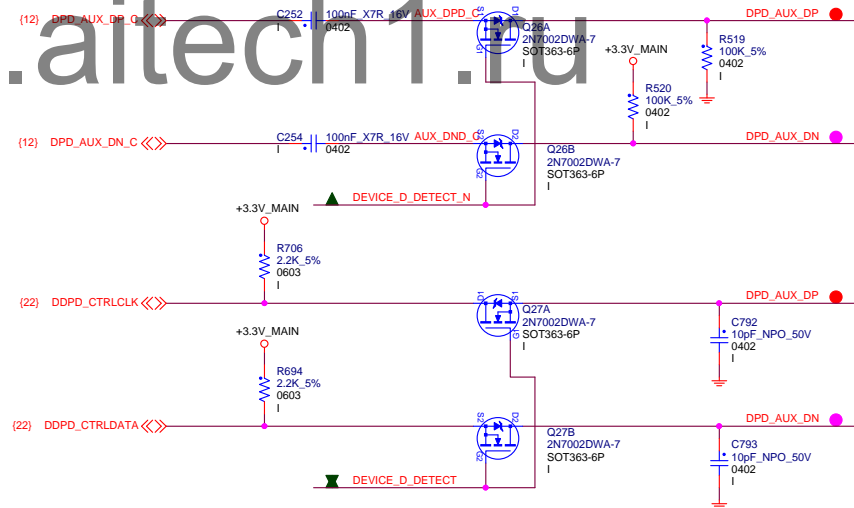
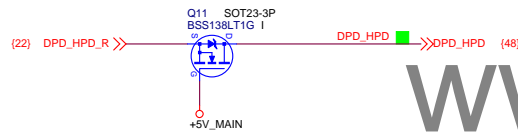
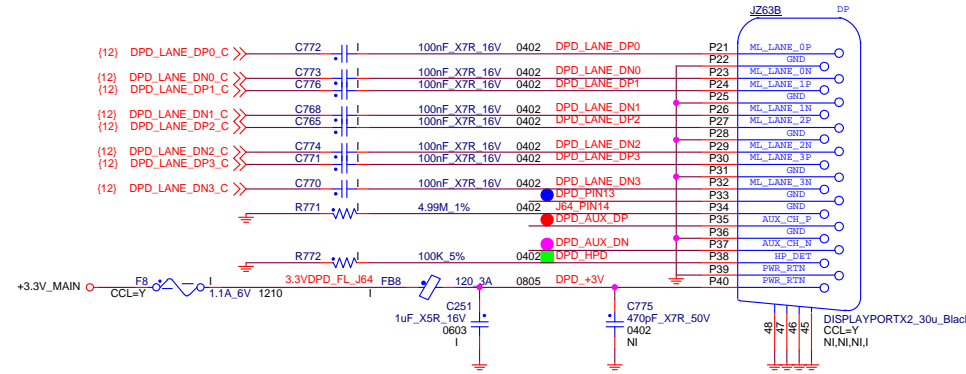
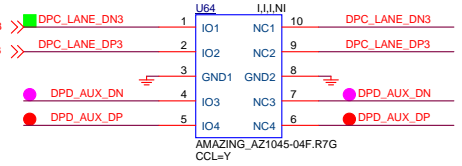
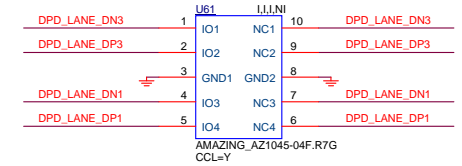
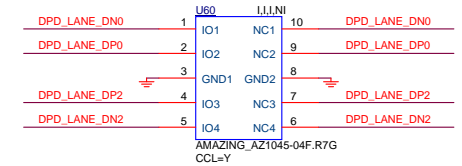
Bunun DP ESD



Bunun DP ESD



ESD suppressor

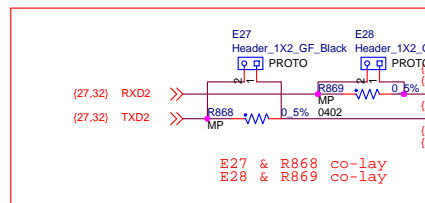


PIN13		FUNCTION
DP	DONGLE	
L	X	DEVICE_D_DETECT
X	H	DEVICE_D_DETECT_N

BOM DISTRIBUTION RULE
Spitfire, Scorpion, Toledo, Z2
(BOM,BOM,BOM, BOM)

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Size	Document Number				Rev
Custom	795207-000				A
Date: Monday, June 29, 2015		Sheet		49	of 72

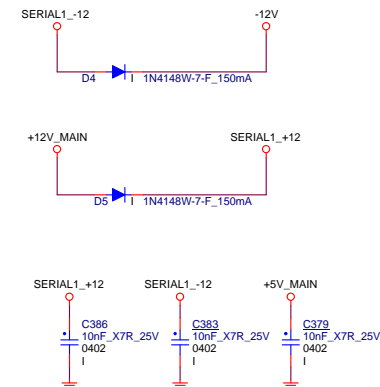
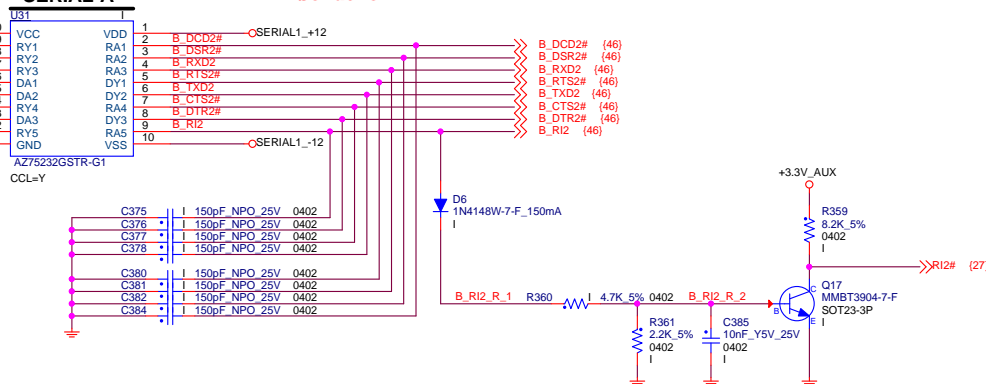


@E27(1-2)
Jumper_2P_GF_Blue
PROTO

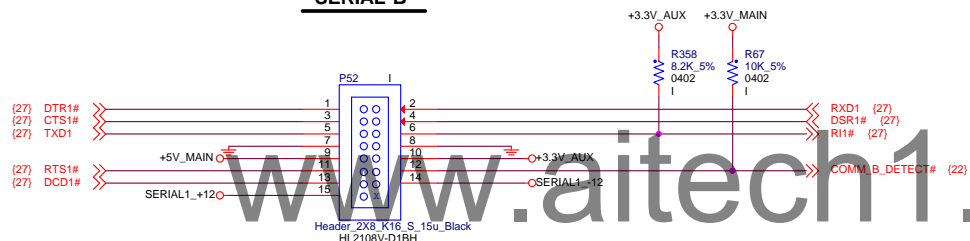
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Jumper_2P_GF_Blue
PROTO

SERIAL A

12V solution



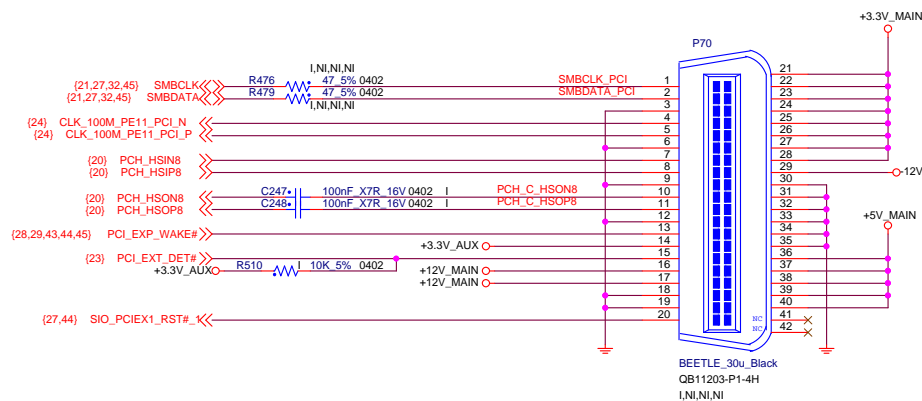
SERIAL B



P52
Serial B

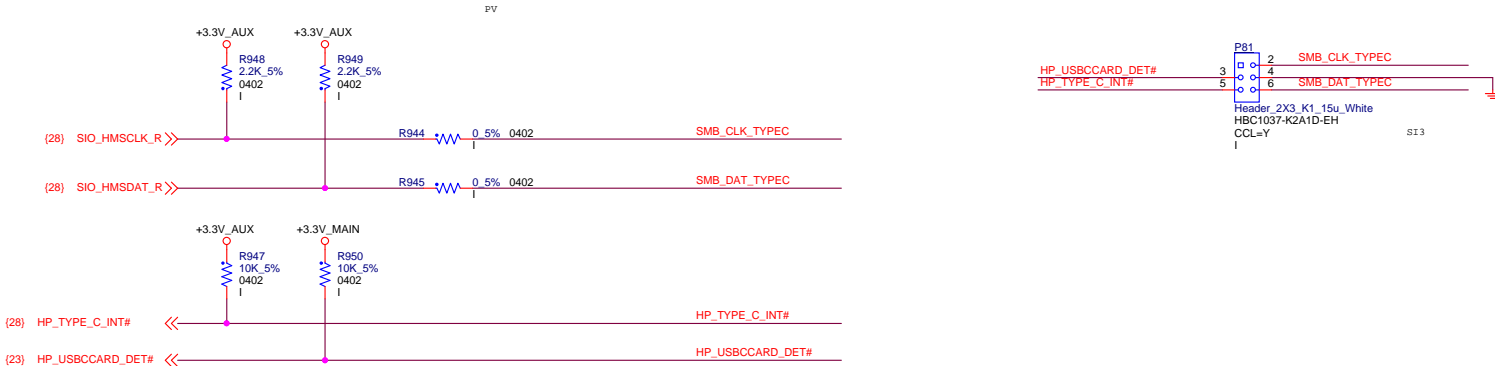
1 COM_DTR1#	2 COM_SDIN1
3 COM_CTS1#	4 COM_DSR1#
5 COM_SDO1	6 COM_RI1#
7 GND	8 GND
9 +5V_SYS	10 +3.3V_SB
11 COM_RTS1#	12 COM_DET#
13 COM_DCD1#	14 -12V_SYS
15 +12V_SYS	16 KEY

SCSI Connector




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Title COMA/COMB/SCSI					
Size	Document Number				Rev
Custom	795207-000				A
Date: Monday, June 29, 2015		Sheet		50	of 72

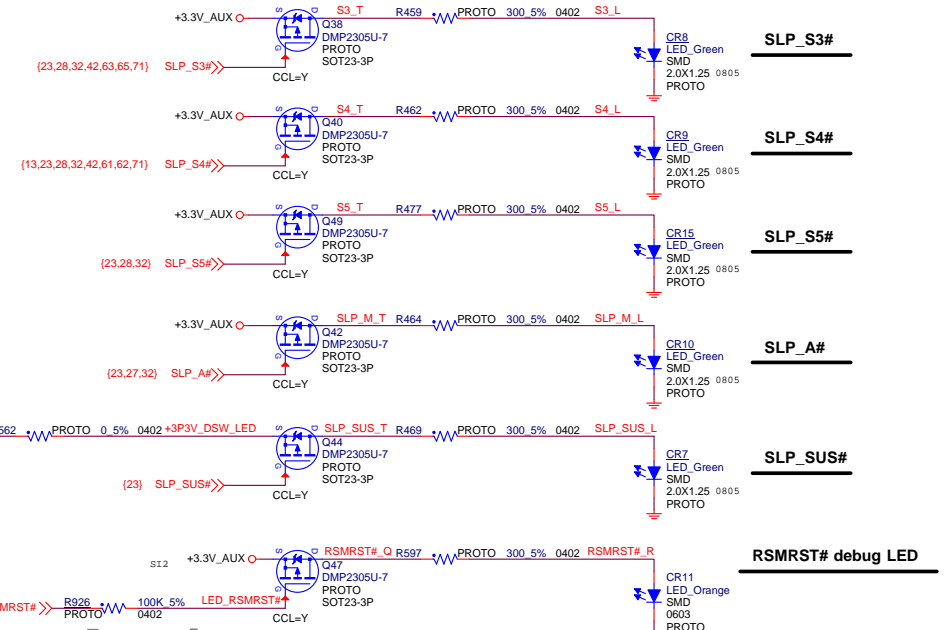
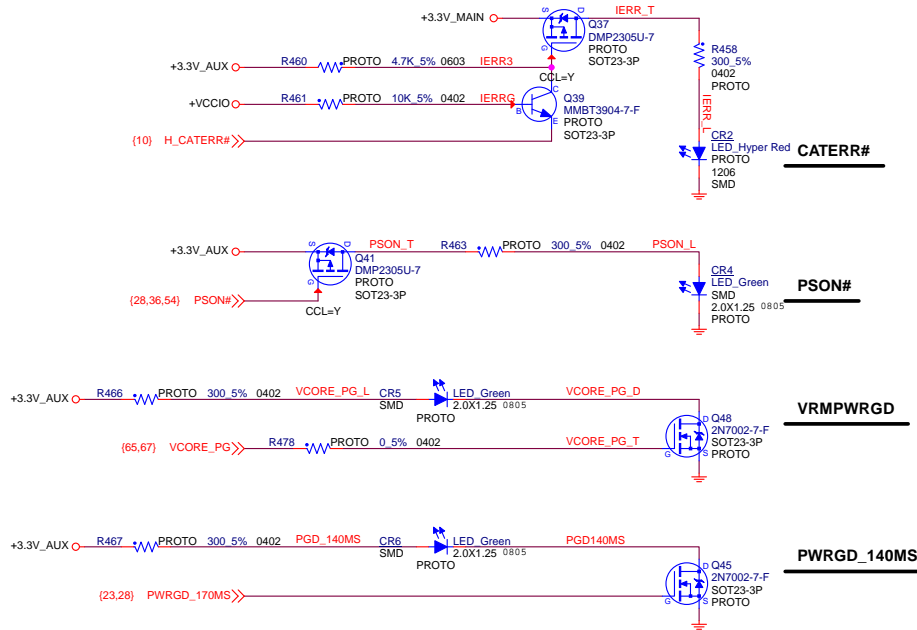


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Size	Document Number				Rev
Custom	795207-000				A
Date: Monday, June 29, 2015		Sheet	51	of	72

PCA LEDs

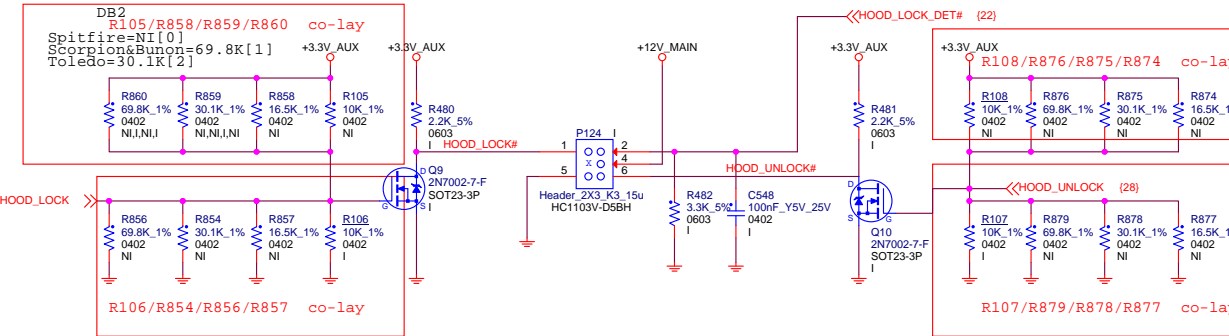


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R105/R106 control ML_STR1 PCA_ID[2:0]

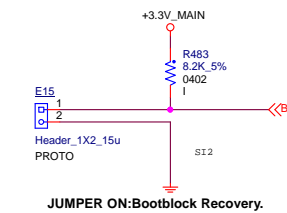
HOOD LOCK CIRCUIT

R108/R107 control ML_STR2 PCA_ID[5:3]



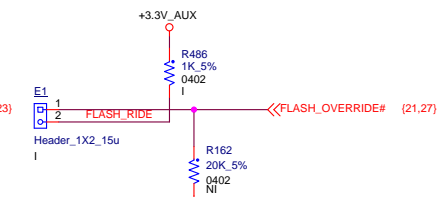
BOOTBLOCK RECOVERY

E15: SPI ROM bootblock recovery header



FLASH OVERRIDE

HDA_SDO: A weak internal pull down. Strap low, the security measures defined in the Flash Descriptor will be in effect (default). Sample high, Flash Descriptor Security will be overridden.

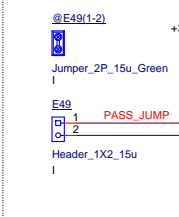


PCA_ID Resistor values

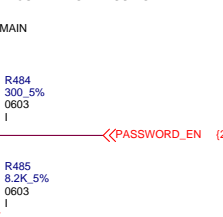
PCA Assignments	PCA_ID	ML_STR2 pin	ML_STR1 pin
SPITFIRE	0	NI	10K
SCORPION/BUNUN	1	NI	10K
TOLEDO	2	NI	10K
	3	NI	10K
	4	NI	10K
	5	NI	10K
	6	NI	10K
	7	NI	10K

PASSWORD JUMPER

Have to take care the location

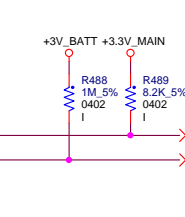


JUMPER ON:PASSWORD ENABLE



HOOD SENSE CIRCUIT

Have to take care the location

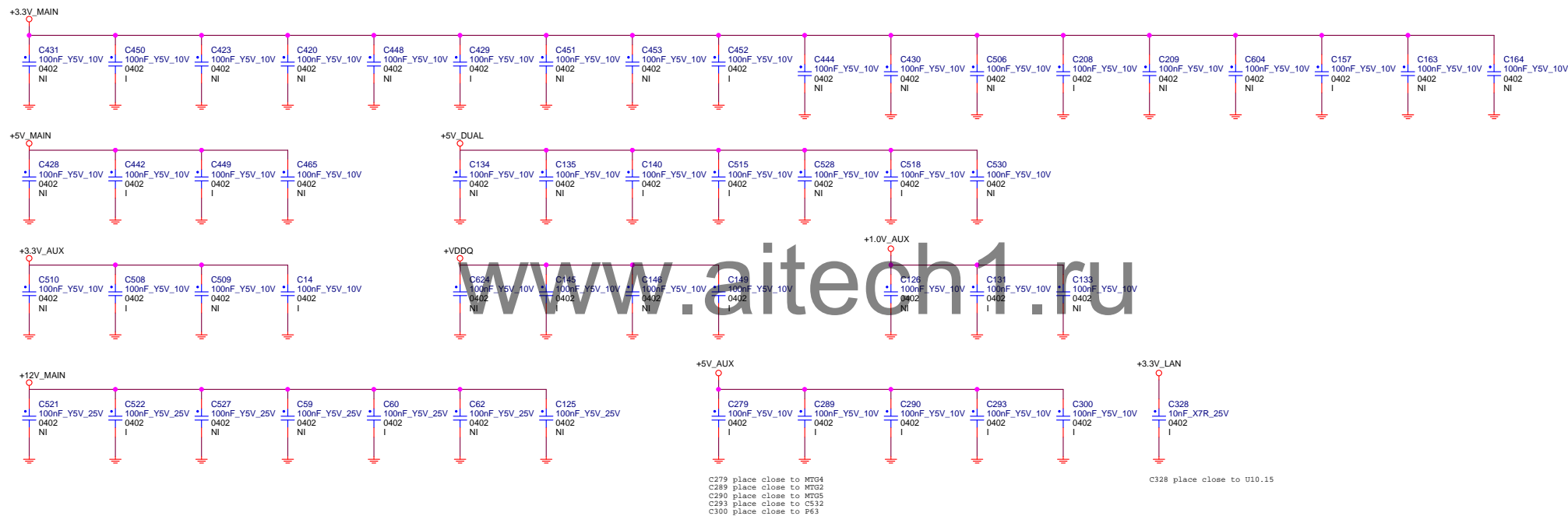


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Spitfire, Scorpion, Toledo, Z2
(BOM,BOM,BOM, BOM)

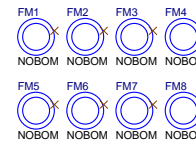
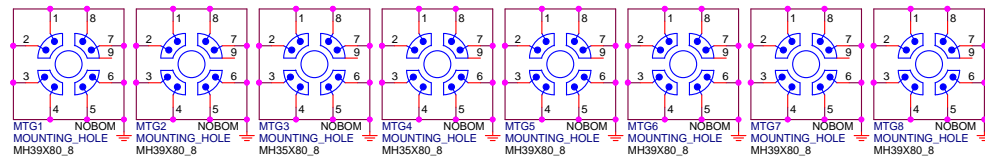
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Custom	795207-000
Date: Monday, June 29, 2015	Sheet 52 of 72
Rev	A

EMI CAP



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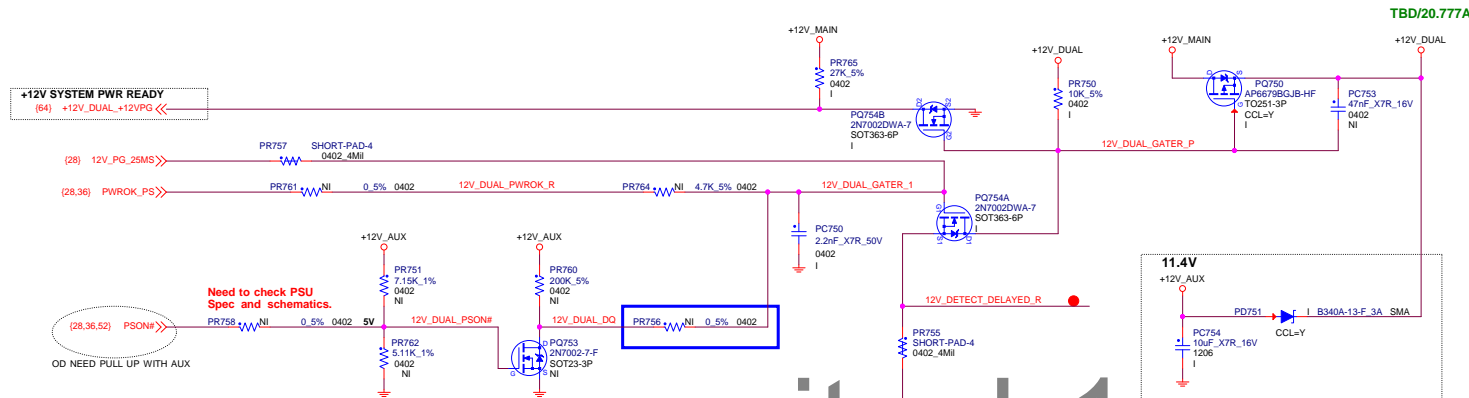


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Custom	795207-000
Date: Monday, June 29, 2015	Sheet 53 of 72
Rev A	

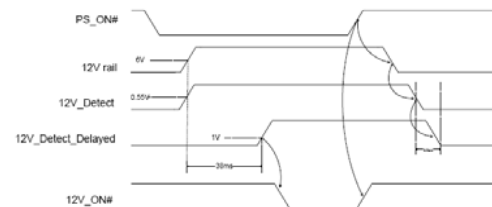
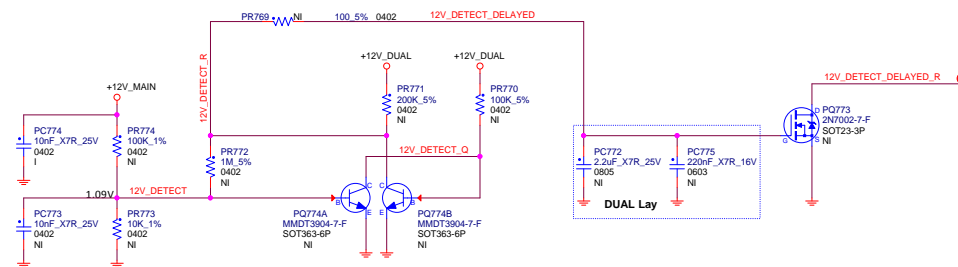
Note: net-name:12V

+12V_DUAL



12V DETECT DELAY CIRCUIT

**PROTO
PARTS**

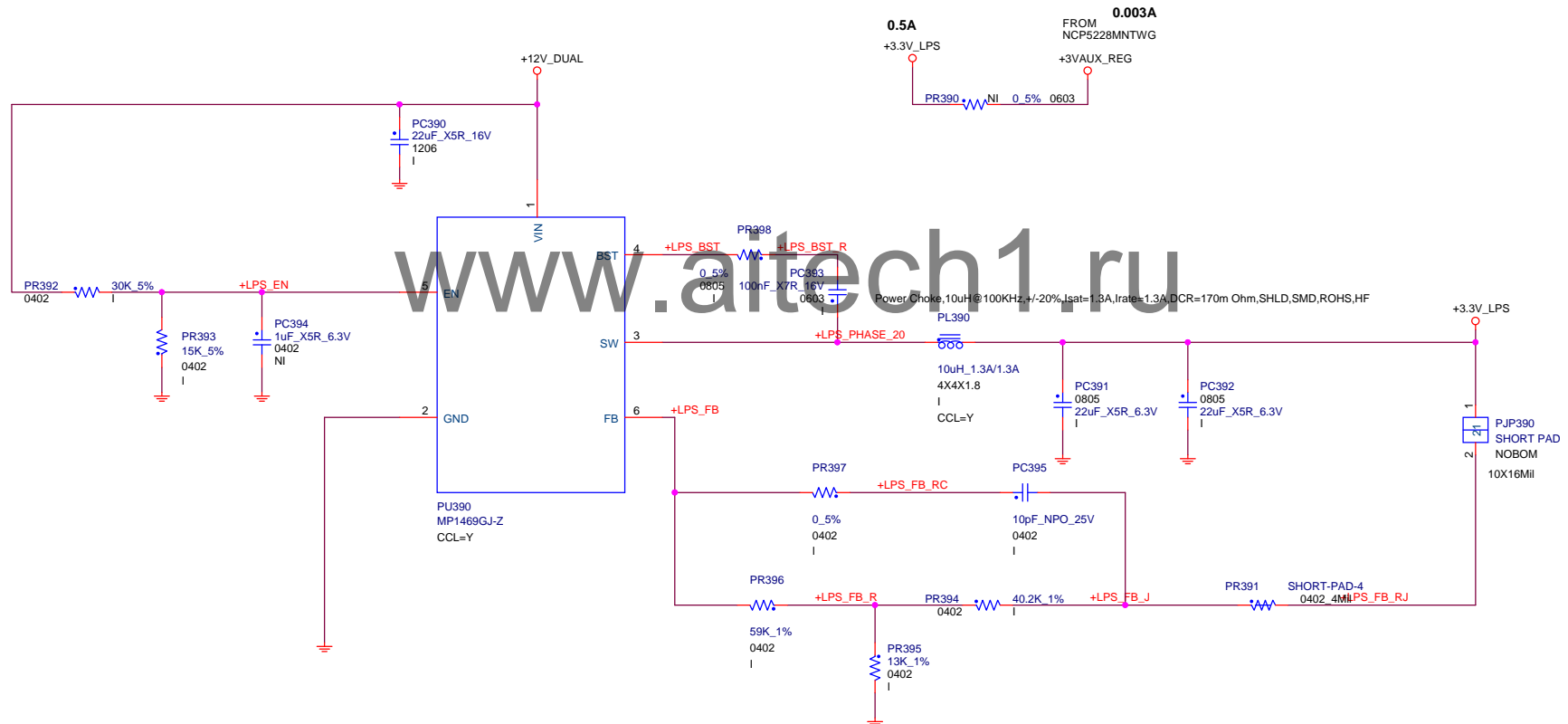


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+3P3V LPS

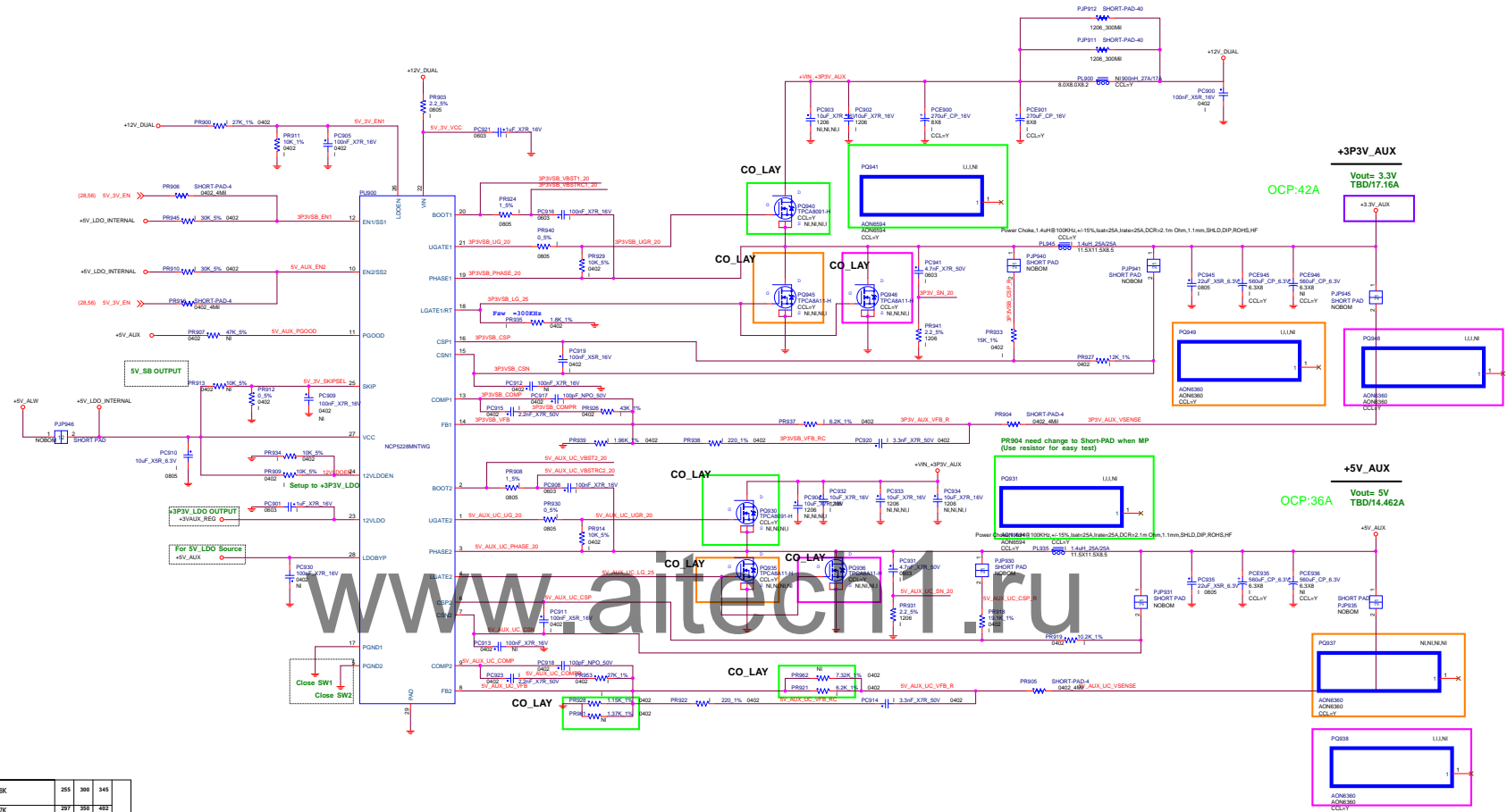
+3P3V_STBY_DSW

Vout= 3.3V
TBD/0.00206A
SO 0.502A



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Date:	Monday, June 29, 2015		Sheet	55	of 72



Switching Frequency	fsw	RLGFS = 1.8K	255	300	345
		RLGFS = 4.7K	397	358	402
		RLGFS = 9.1K	348	408	460
		RLGFS = 10K	519	600	690

RT8122 Truth Table

LDEN	1VLDEN	EN1	EN2	1VLD0	Vcc(+5V)	Vout1	Vout2
L	L	X	X	L	L	L	L
L	2.5V/5V	X	X	3.3V/12V	L	L	L
H	L	X	L	L	H	H	L
H	L	L	L	L	H	L	L
H	2.5V/5V	H/L	H/L	3.3V/12V	H	H/L	H/L
H	2.5V/5V	H/L	H/L	3.3V/12V	H	H/L	H/L

NCF5228 Truth Table

LDEN	1VLDEN	EN1	EN2	1VLD0	Vcc(+5V)	Vout1	Vout2
L	X	X	X	L	L	L	L
L	2.5V/5V	X	X	L	L	L	L
L	2.5V/5V	H/L	H/L	3.3V/12V	H	H/L	H/L
H	2.5V/5V	H/L	H/L	3.3V/12V	H	H/L	H/L

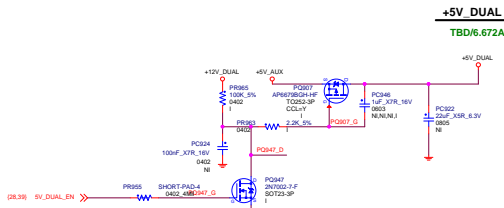
System Power Control Signal Truth Table

	LPS	S5	S3	S0
5V_3V_EN	L	X	X	X
3P3V5B_EN	L	H	H	H
5V_DUAL_EN	X	L	H	H

X: floating

System Power State Truth Table

	LPS	S5	S3	S0
+5V_ALW	H	H	H	H



+3.3V_AUX Bleed off Circuit

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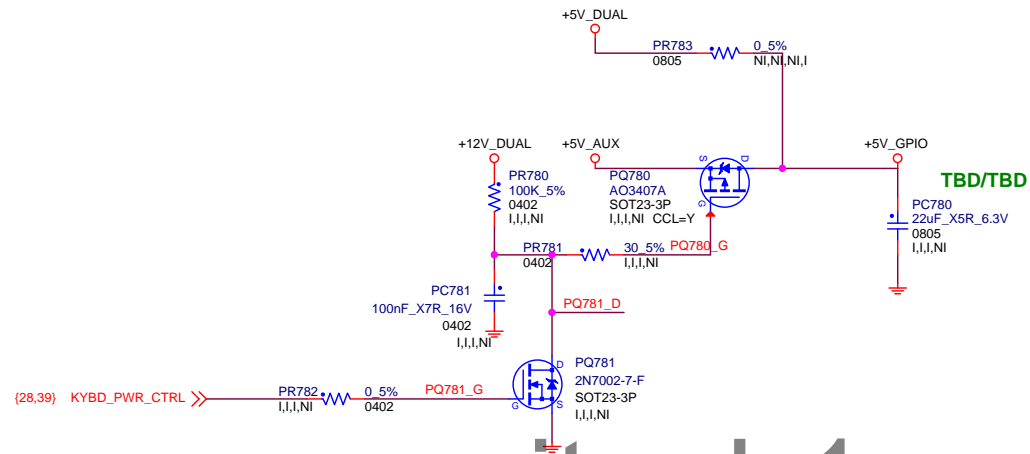
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Sheet: 56 of 72



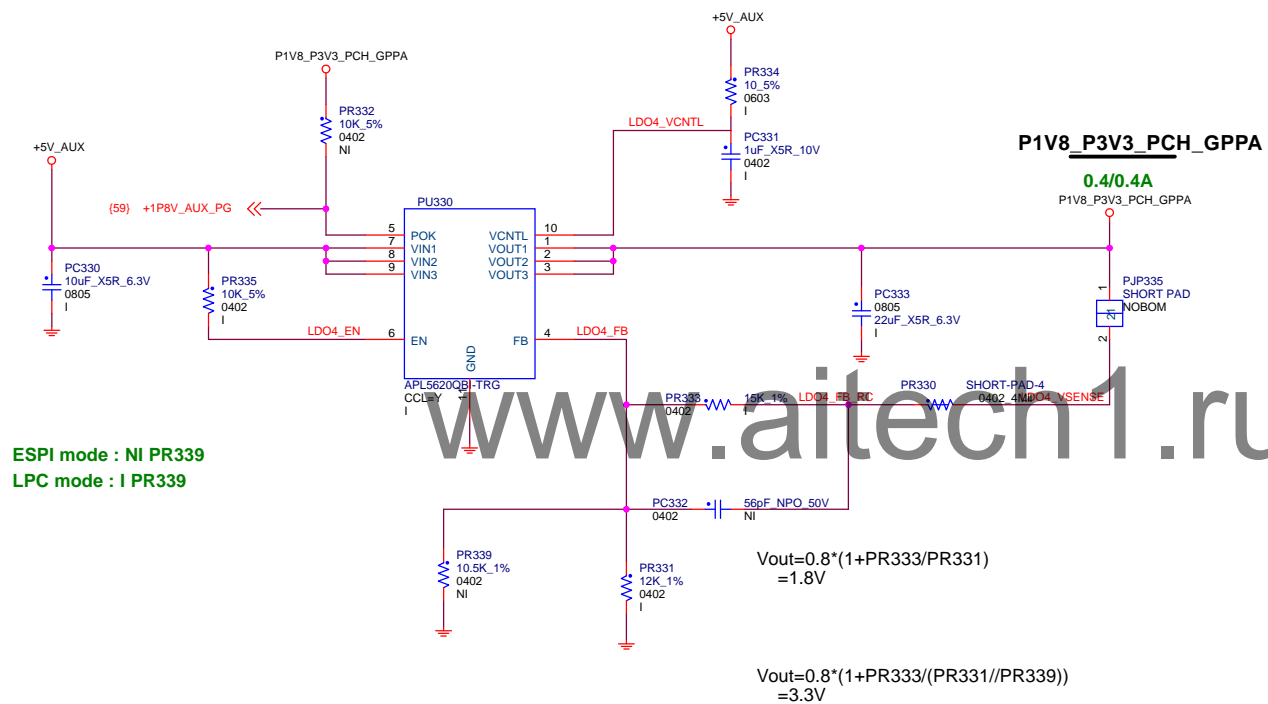
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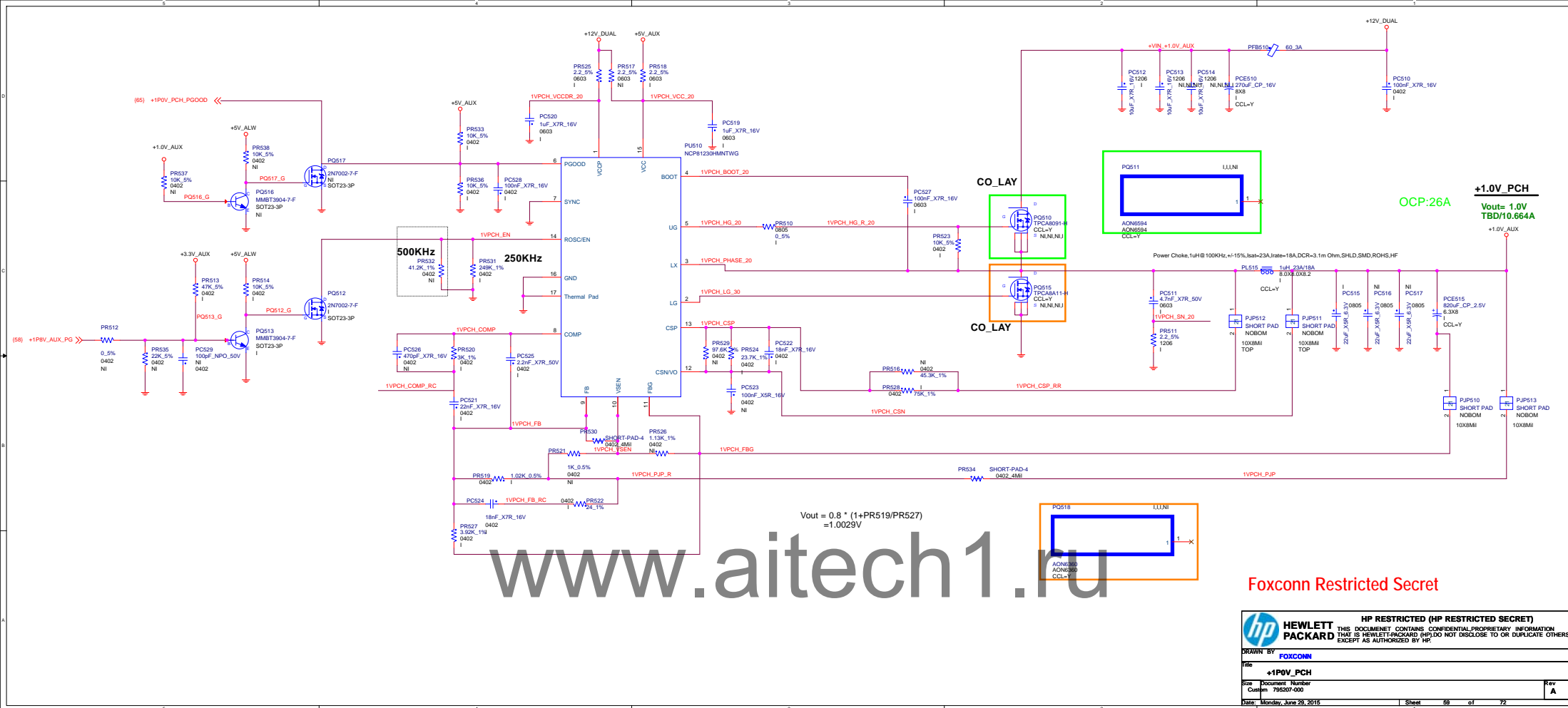
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P1V8_P3V3_PCH_GPPA

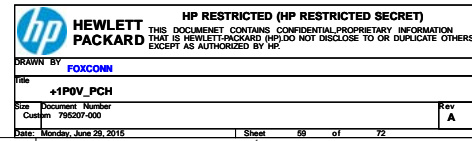


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Custom	795207-000		
Date:	Monday, June 29, 2015	Sheet 60 of 72	

PR570 set frequency
 $f_{sw} \text{ (KHz)} = 38000 \times V_o / R_{ton} \text{ (kohm)}$
 $= 500K$

+VPP
 $V_{out} = 2.5V$
 $TBD/2.24A$

PC579 should near XMM1


$T_{ss}(\mu s) = 330 \times C_{ss}(nF)$
 $= 3.3ms$

$V_{out} = 0.8 \times (1 + PR565/PR568)$
 $= 2.52V$

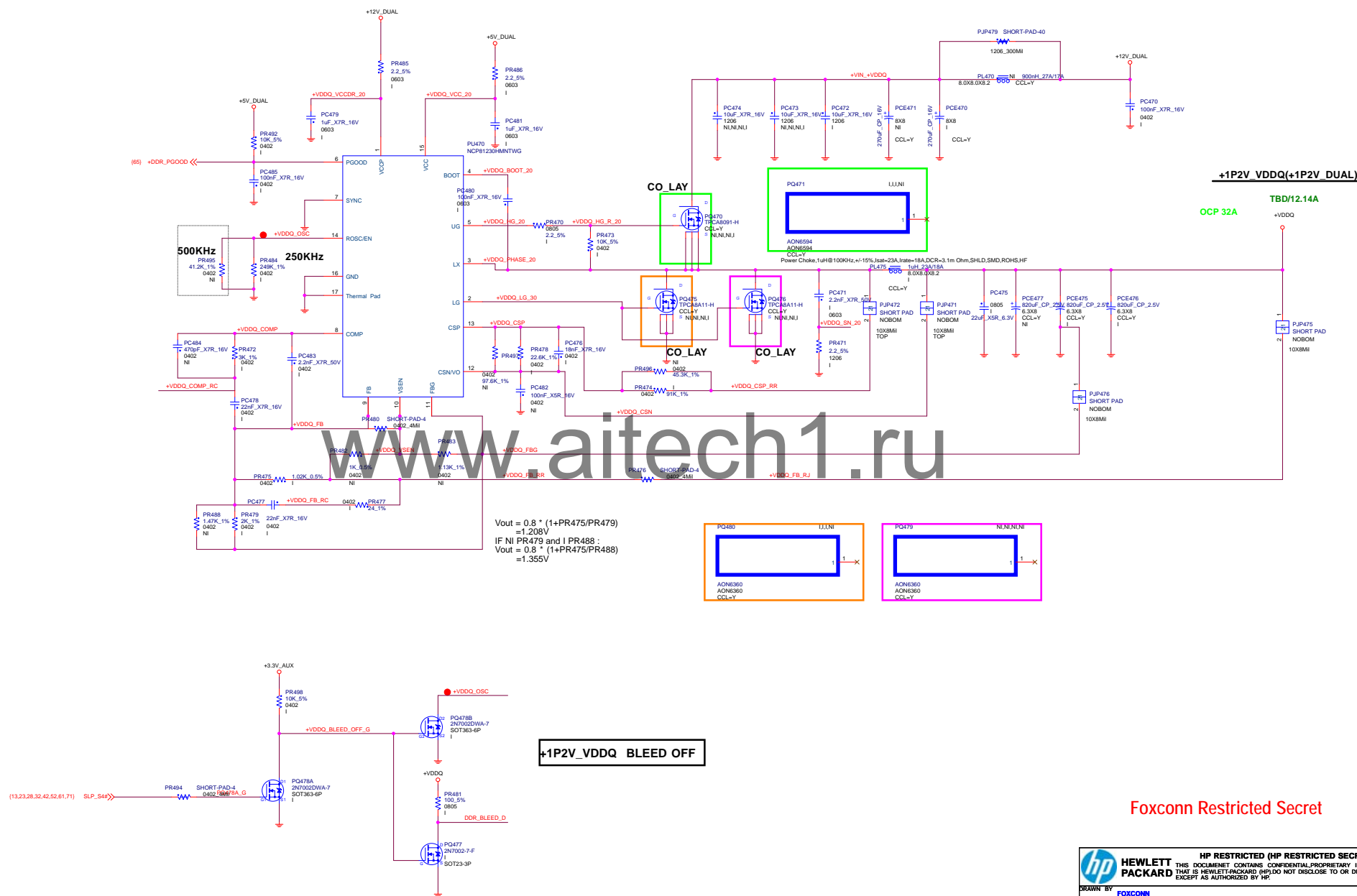
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$V_{out} = 0.8 \times (1 + PR633/PR632)$
 $= 2.61V$

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Pcs: +VPP			
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Date: Monday, June 29, 2015		Sheet: 61 of 72	

+1P2V_VDDQ



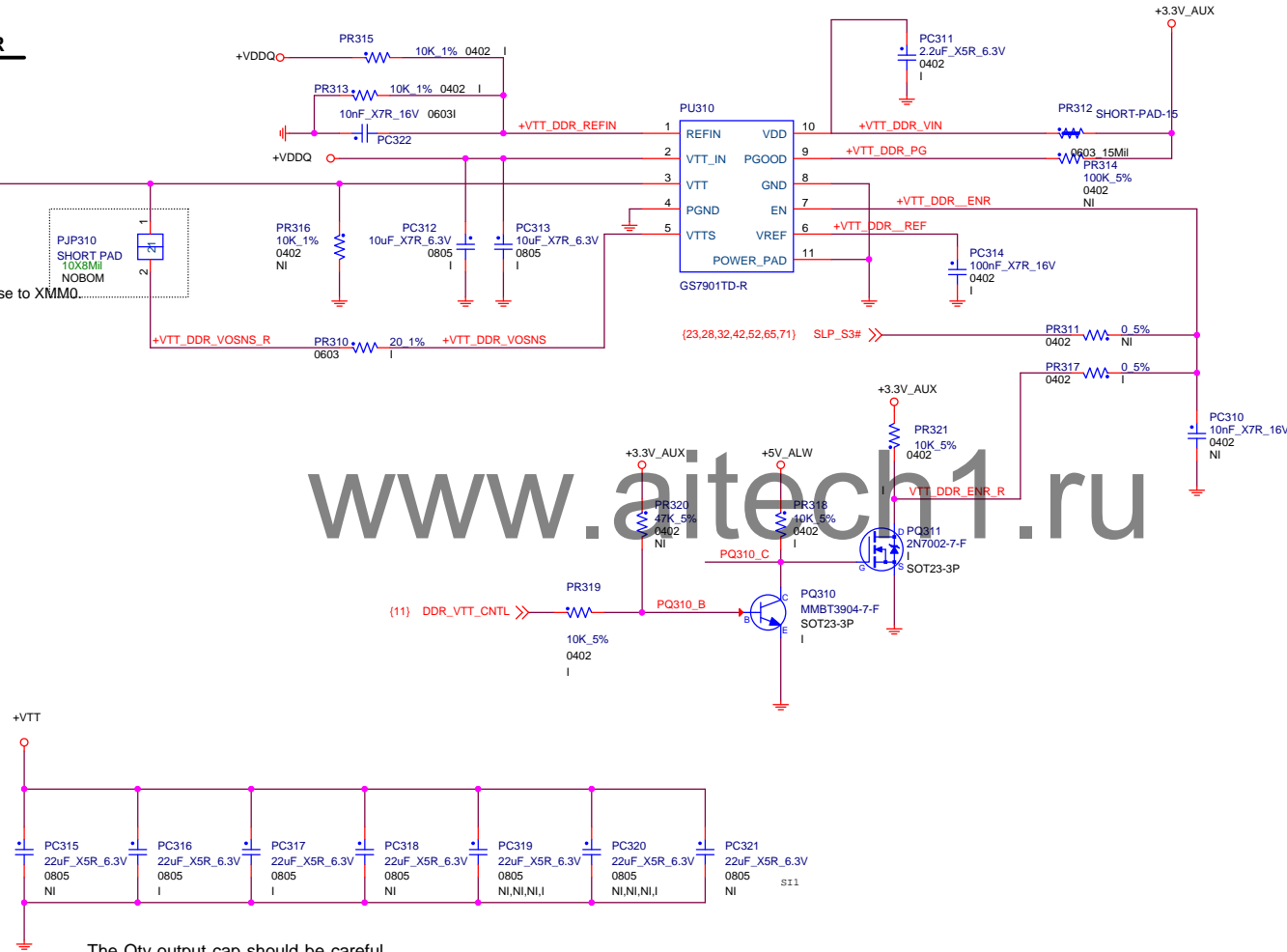
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DDR_VTT

+VTT_DDR

TBD/2.5A

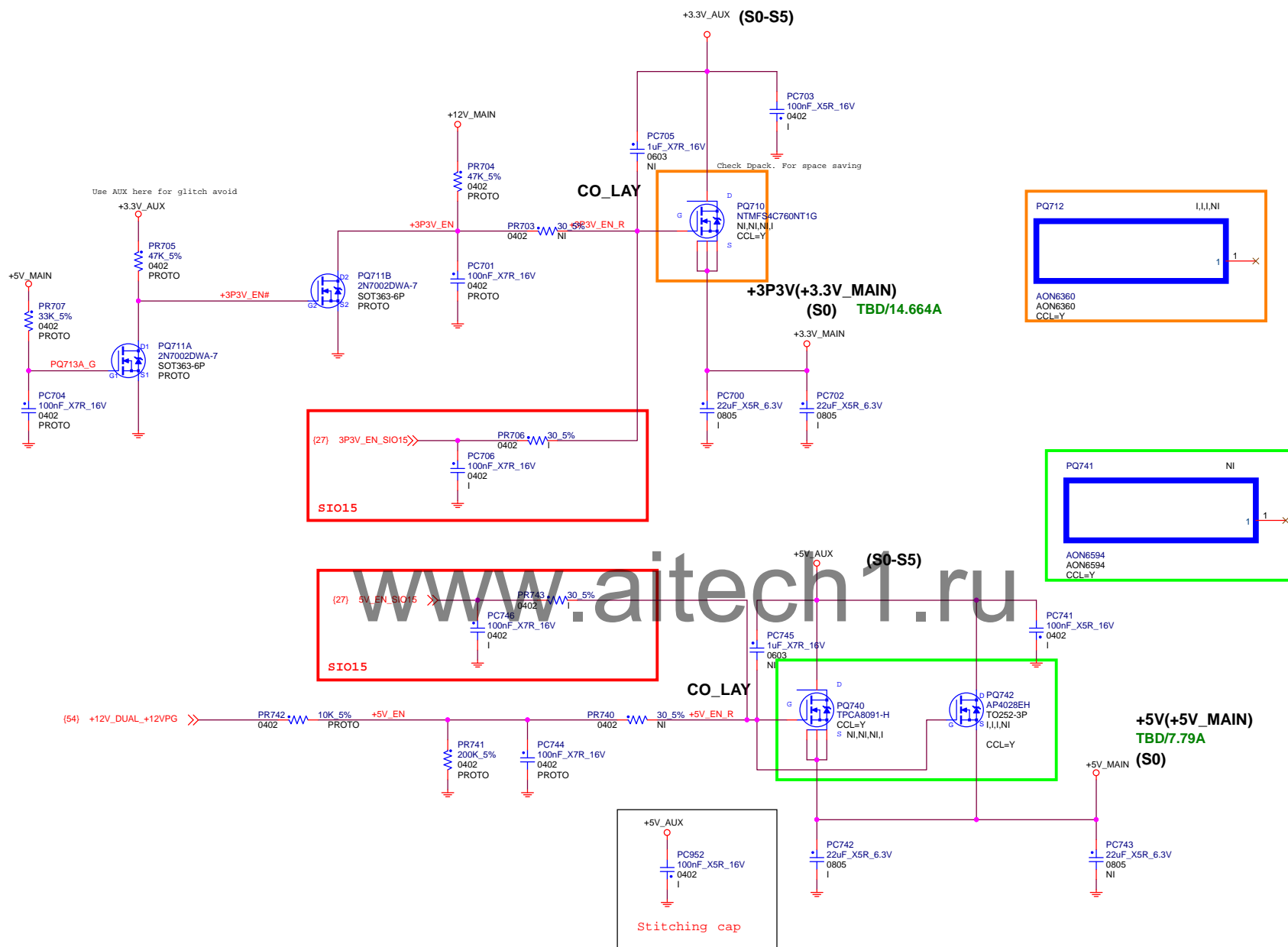
Note:PJP310 close to XMM0.



The Qty output cap should be careful
INTEL: the latest modeling shows step load size 6-9x higher than it's shown in PDG
1.0 for Aztec City CRB

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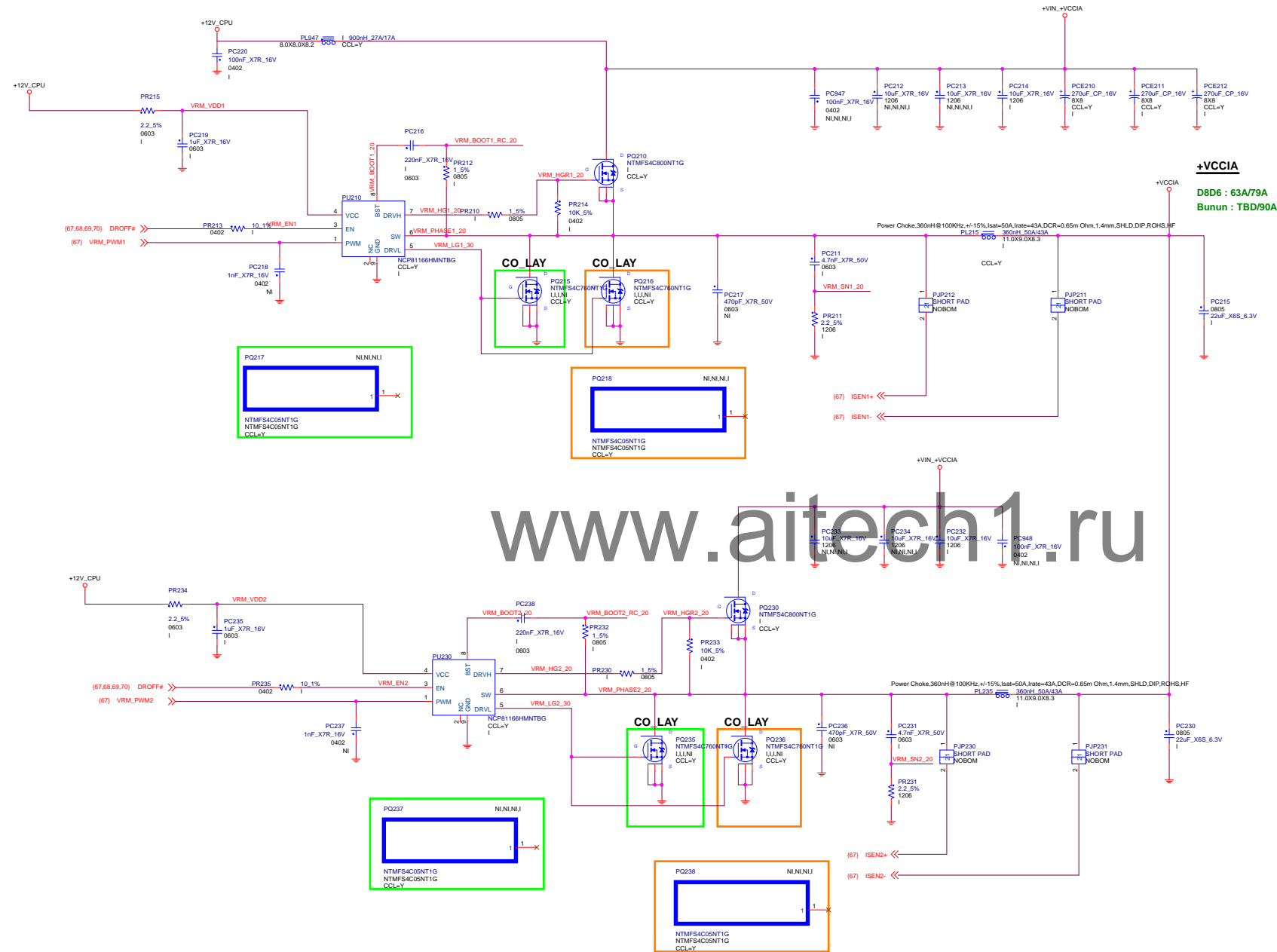
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Custom	795027-000	A
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VCORE PHASE1~2




+VCCIA

D8D6 : 63A/79A
Bunun : TBD/90A

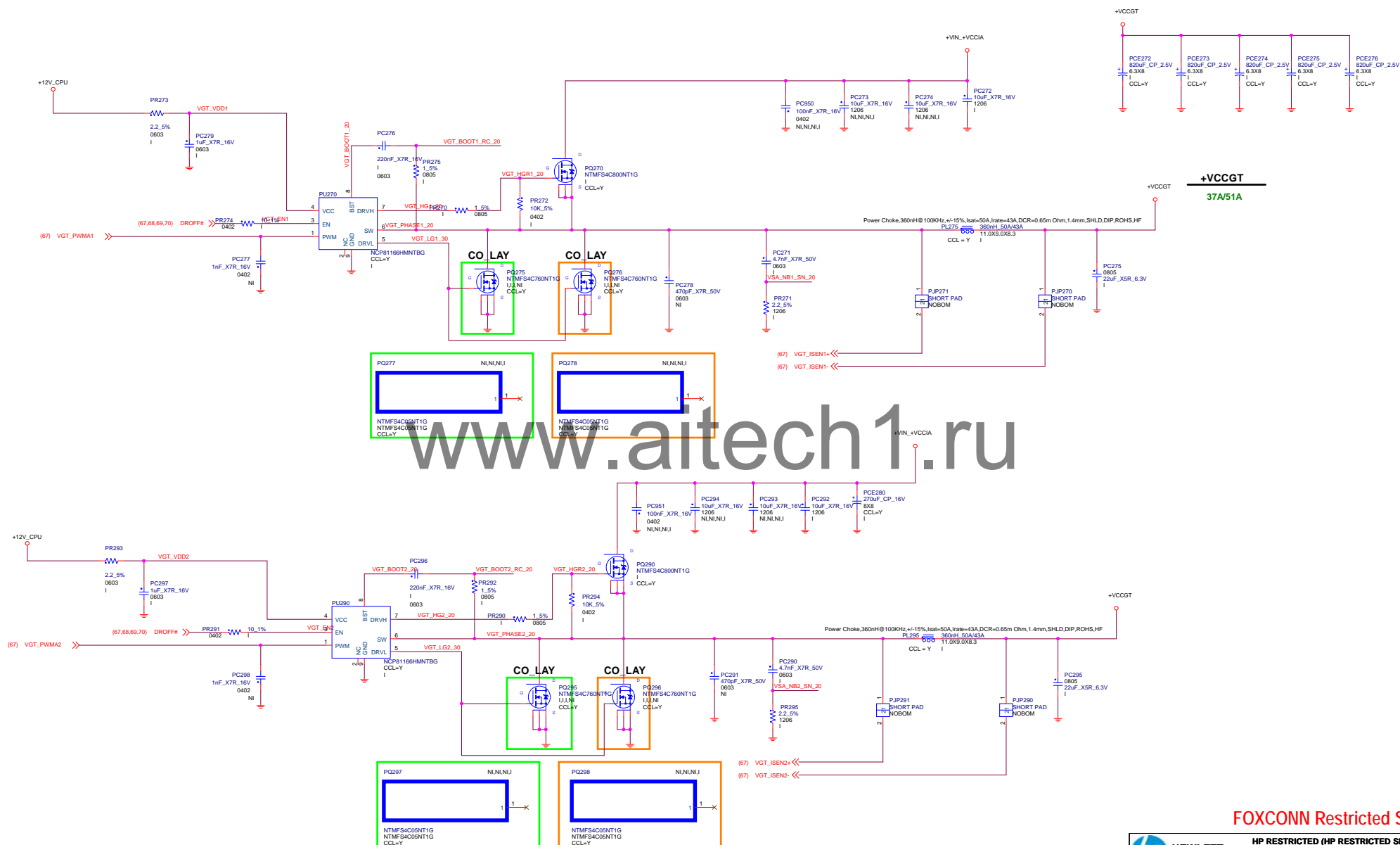
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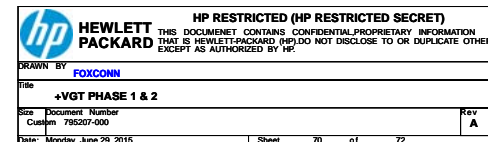
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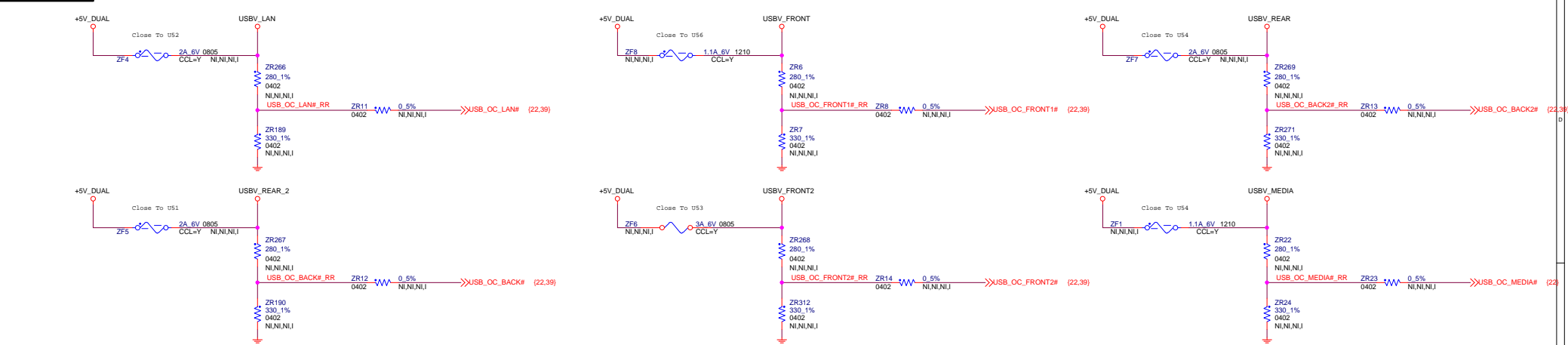
VGT PHASE1~2



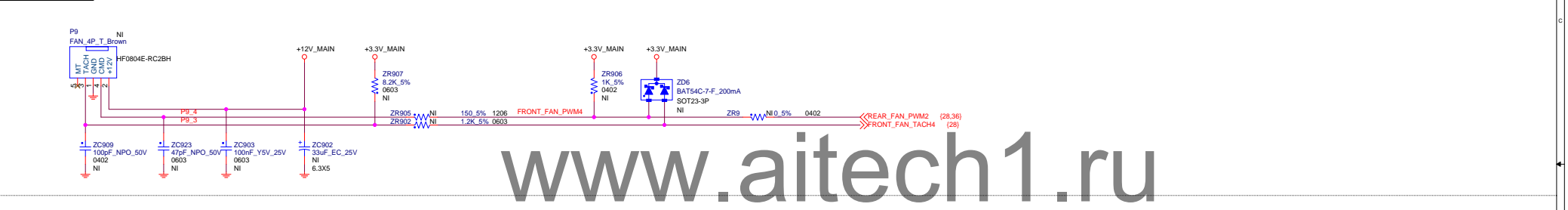
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USB POWER

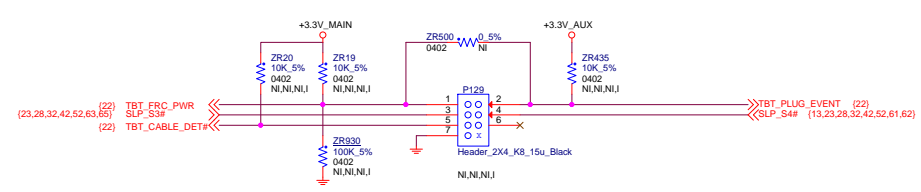


FRONT CHASIS

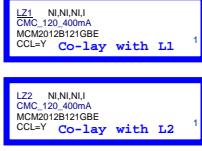


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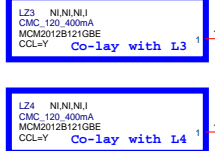
Z2 ThunderBolt



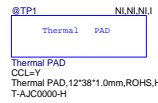
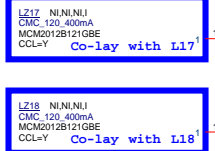
Bunun J9 USB2.0 CMC



Bunun JZ10 USB2.0 CMC



Bunun Front USB2.0 CMC



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